10 / Bipolar Process Integration

In this chapter, interactions between fabrication processes and bipolar device design and layout will be explored. In particular, we will look closely at relationships between impurity profiles and device parameters such as current gain, transit time, and breakdown voltage. The use of recessed oxidation and self-aligned processes in the formation of high-performance bipolar transistors will be presented, and design rules for bipolar structures will also be discussed. In conclusion, collector-diffusion, V-groove, and dielectric isolation processes will be discussed.

10.1 THE JUNCTION-ISOLATED STRUCTURE

The basic junction-isolated bipolar process of Fig. 10.1a has been used throughout the IC industry for many years and has become known as the *standard buried collector* (SBC) process. In this junction-isolated process, adjoining devices are separated by back-to-back *pn* junction diodes which must be reverse-biased to ensure isolation (see Fig. 10.1b). The SBC process remains the primary bipolar process for analog and power circuit applications with power supplies exceeding 15 V. Although the SBC process was also originally used for logic circuits, most digital technologies have evolved to self-aligned, oxide-isolated processes using polysilicon and other technology advances first developed for MOS processes.

The process flow for the SBC structure of Fig. 10.1a was discussed in Section 1.4 and will only be outlined here. An n^+ buried layer is formed by selective diffusion into a ⟨111⟩-oriented *p*-type substrate and is followed by growth of an *n*-type epitaxial layer. Isolated *n*-type collector islands are formed using a deep boron diffusion. The base and emitter are formed by successive *p*- and *n*-type diffusions into the epitaxial layer. The structure is completed with contact window formation and metallization.

A cross section of the SBC impurity profile through the center of the device is shown in Fig. 10.2. In the next several sections we will consider how the design of this profile is related to several important measures of device performance. An understanding of the basic profile design for the SBC process will help us see the advantages and disadvantages of other types of processes.

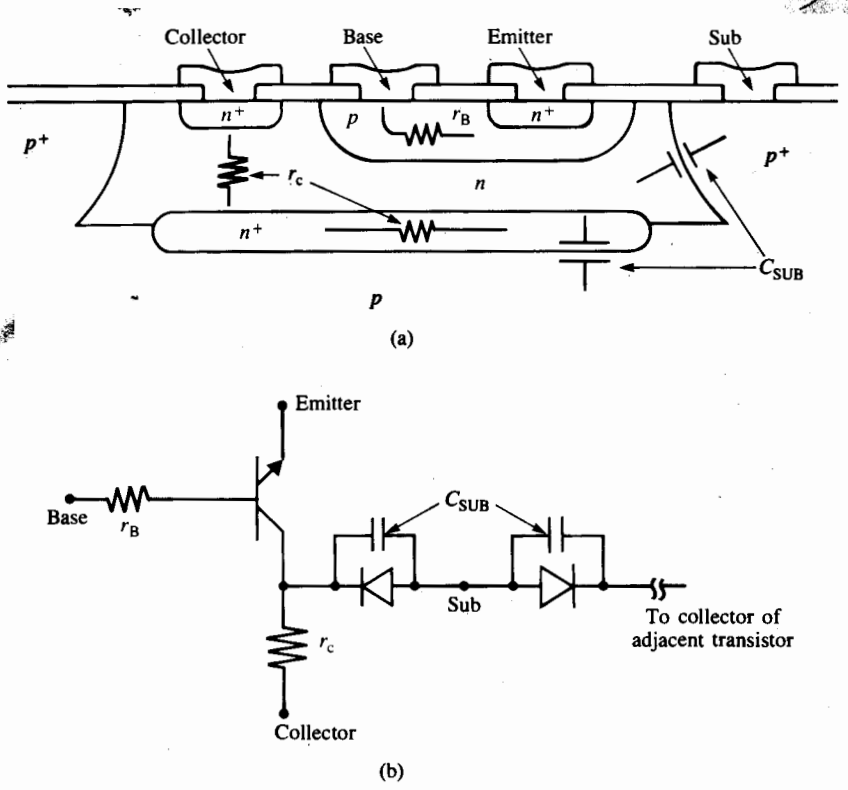


Fig. 10.1 (a) Cross section of a transistor fabricated with the SBC process showing the collector-base capacitances and the base and collector series resistances; (b) lumped circuit model for the transistor showing back-to-back diodes which provide isolation between adjacent transistors.

10.2 CURRENT GAIN

In order to be useful in circuits, the bipolar transistor must have a current gain of at least 10 to 20 for digital applications and an order of magnitude greater for analog applications. An expression for the current gain of the bipolar transistor is

$$\beta^{-1} = \frac{(N_B/D_B)}{(N_E/D_E)} + \frac{W_B^2}{\eta L_B^2} \tag{10.1}$$

The basewidth, W_B, is the width of the electrically neutral base region of the transistor. The constant η is determined by the shape of the impurity profile in the base and ranges from 2 to 20. L_B is the diffusion length for minority carriers in the base. D_E and D_B are the effective minority-carrier diffusion constants in the emitter and the base, respectively.

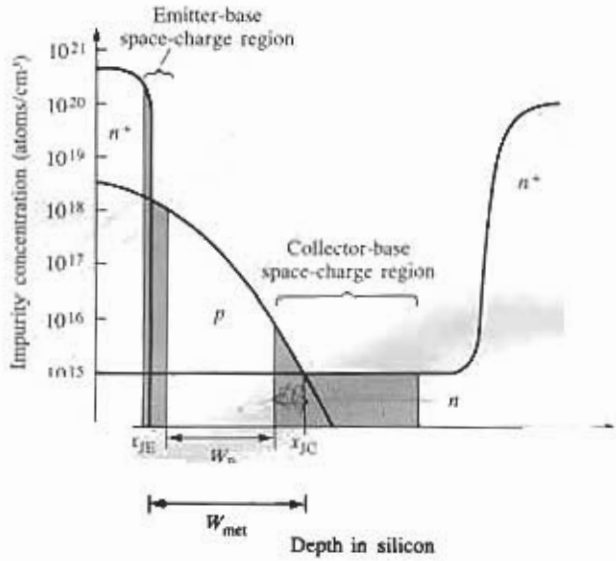


Fig. 10.2 Vertical impurity profile in typical bipolar junction transistor. The shaded regions represent the emitter-base and collector-base space-charge regions. The metallurgical basewidth and electrical basewidth are indicated by W_{met} and W_B, respectively.

N_B and N_E are the *Gummel numbers* in the base and emitter, defined by

$$N_B = \int_{\text{base}} N(x)\,dx \quad \text{and} \quad N_E = \int_{\text{emitter}} N(x)\,dx \tag{10.2}$$

and represent the impurity dose in the base and emitter regions. Heavy doping effects in the emitter typically limit the value of N_E/D_E to 10^{13} to 10^{14} sec/cm^4. The basewidth is defined by the distance between the edges of the two space-charge regions in the base. For wide-base transistors, this is approximately equal to the distance between the metallurgical junctions as shown in Fig. 10.2. For narrow-base transistors, the space-charge regions must be subtracted from the metallurgical basewidth, as discussed further in Section 10.4.

For large current gain, eq. (10.1) should be as small as possible. The ratio of the Gummel numbers in the base and emitter should be low, the width of the base region should be small, and L_B should be large. Figure 10.3 shows the dependence of the diffusion length on impurity concentration. As the doping level increases, L_B decreases, but is greater than 10 μm for typical base-doping concentrations. In modern high-frequency transistors, the basewidth W_B is typically much less than the diffusion length L_B, and the first term in eq. (10.1) determines the current gain.

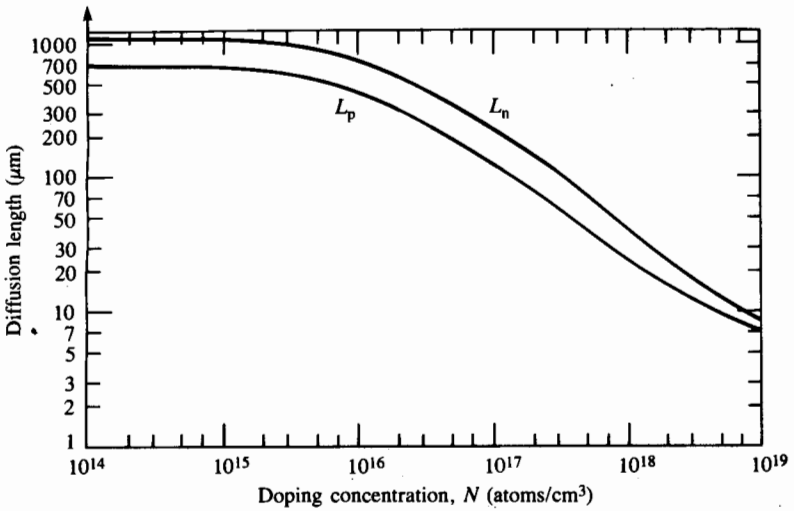


Fig. 10.3 Calculated minority-carrier diffusion lengths as a function of doping concentration for bulk silicon using lifetime equations from ref. [1].

From eqs. (10.1) and (10.2), the emitter must be heavily doped relative to the base in order to obtain high gain. In fabricating a bipolar transistor, each successive diffusion is heavier than the last, and the final n^+ diffusion naturally performs best as the emitter.

Example 10.1: Estimate the current gain for a transistor with the following parameters: $N_E/D_E = 5 \times 10^{13}$ sec/cm^4, $N_B/D_B = 10^{12}$ sec/cm^4, $W_B = 1$ μm, $L_B = 20$ μm, and $\eta = 10$.

Solution: Plugging these parameters into eq. (10.1) yields $\beta^{-1} = 0.02 + 0.00025$ and $\beta = 50$. In this transistor, the current gain is dominated by the ratio of the Gummel number terms.

10.3 TRANSIT TIME

Another important bipolar device parameter is the delay incurred during carrier propagation between the emitter and collector terminals of the transistor. Both logic switching speed and amplifier frequency response are limited by the *transit time,* which is defined by

$$\tau = \frac{W_B^2}{\eta D_B} + (C_{JC} + C_{sub})r_C + X_C/2V_S \tag{10.3}$$

The unity-gain frequency of the transistor, f_T, is given approximately by

$$f_T = 1/2\pi\tau \tag{10.4}$$

The first term in eq. (10.3), called the *base transit time,* represents the time required for a carrier to move across the neutral base region W_B. The second term is the delay associated with charging the capacitances connected to the collector node through the collector series resistance r_C. The capacitances C_{JC} and C_{sub} are determined by the collector-base and collector-substrate junction areas and by the doping concentrations of the base, collector, and substrate regions. The third term is the delay time associated with a carrier crossing the depletion region of the collector-base junction. X_C is the width of the depletion layer and V_S is the saturation velocity of the carriers.

In order to minimize τ, the basewidth is made as narrow as possible, the buried layer is added to minimize the value of r_C, and light doping is used to minimize the capacitances. Estimates of the capacitance of the junctions can be made using the one-sided step-junction expression (eq. 9.3), in which the capacitance is determined by the concentration on the lightly doped side of the junction.

Example 10.2: Calculate the transit time for a bipolar transistor with the following parameters: $W_B = 1\ \mu m$, $\eta = 10$, $D_B = 20\ cm^2/sec$, $C_{JC} + C_{sub} = 2$ pF, $r_C = 250$ ohms, $X_C = 10\ \mu m$, and $V_S = 10^7$ cm/sec.

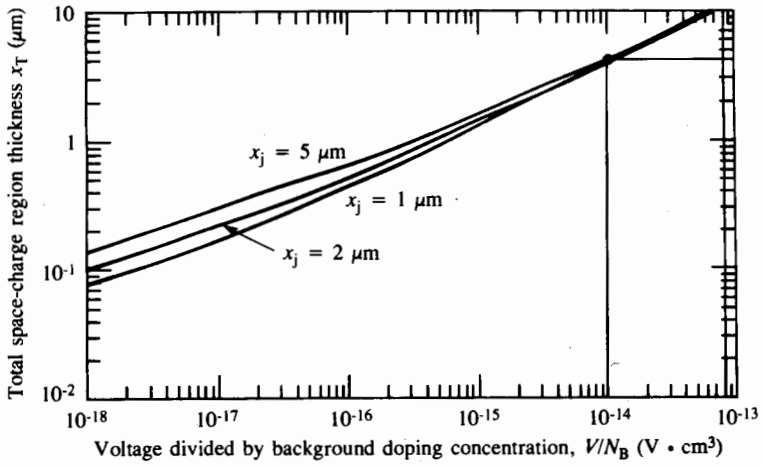
Solution: Plugging these values into eq. (10.3) gives the following values for the three terms: (i) 0.05×10^{-9} sec; (ii) 0.5×10^{-9} sec; (iii) 0.05×10^{-9} sec. The resulting value of transit time is 0.60×10^{-9} sec. The unity-gain frequency f_T is equal to 265 MHz.

10.4 BASEWIDTH

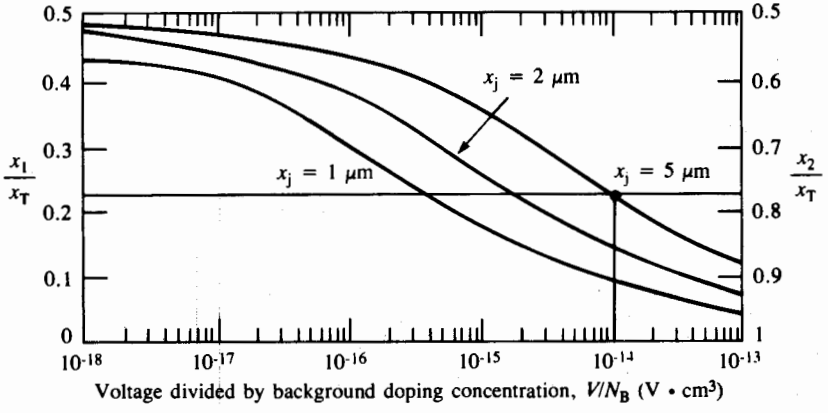
Eqs. (10.1) through (10.3) indicate that device performance is improved by making the basewidth as narrow as possible. The primary restrictions on reducing the basewidth are set by breakdown-voltage requirements and by tolerances on the basewidth due to variations in process control. For low-voltage logic devices, the metallurgical basewidth may be less than 1 μm. For higher-voltage devices used in analog circuit or power applications, the basewidth must be wide enough to support the collector-base depletion-layer width under large reverse bias.

The actual basewidth of the transistor is determined by reducing the metallurgical basewidth by the portions of the emitter-base and collector-base space-charge regions which protrude into the base, as shown in Fig. 10.2. The emitter and base are both heavily doped near the junction, and although the space-charge-region width of the emitter-base junction is usually quite small, it does extend almost entirely into the base. Its width can be estimated from Fig. 9.4.

The collector-base space-charge region width is dependent on the voltage across the junction and extends into both the base and collector regions. Figure 10.4 shows the depletion-layer width on either side of a *pn* junction formed by a Gaussian diffusion into a uniformly doped substrate, the normal situation for a bipolar transistor fabricated using the SBC process.



(a)



(b)

Fig. 10.4 The space-charge region width as a function of voltage and doping for a *pn* junction formed by a Gaussian diffusion into a uniformly doped substrate. (a) Total space-charge region width x_T; (b) fraction of total space-charge region width extending on the heavily doped side, x_1, and on the lightly doped side, x_2, respectively. After ref. [4]. Reprinted with permission from the *AT&T Technical Journal*. Copyright 1960 AT&T.

Example 10.3: Estimate the space-charge region widths on each side of the collector-base junction of a bipolar transistor fabricated on a 1-ohm-cm *n*-type epitaxial layer. The reverse-bias voltage across the junction is 40 V, and the collector-base junction depth is 5 μm.

Solution: The doping of the epitaxial layer is $4 \times 10^{15}/\text{cm}^3$, giving a value of $V/N_B = 1 \times 10^{-14}$ V-cm³. From Fig. 10.4a, the total depletion-layer width is approxi-

mately 4 μm. From Fig. 10.4b, 77% or 3.1 μm extends into the collector region, and 23% or 0.9 μm extends into the base region.

Heavy base doping reduces the size of the space-charge regions in the base, permitting a narrow-base design. However, heavy base doping tends to increase the Gummel number in the base, which reduces the current gain of the transistor. Heavy doping also increases the collector-junction capacitance, thus increasing the transit time in eq. (10.3). This is another situation in which conflicts arise when trying to optimize several different device parameters simultaneously.

10.5 BREAKDOWN VOLTAGES

The process designer must understand the magnitude of the voltages that will be applied to the transistors in circuit applications. The device in Example 10.3 had to withstand 40 V and was probably designed for analog-circuit applications. On the other hand, transistors designed for logic applications must support only relatively low voltages. For example, the devices used in TTL circuits are designed to withstand only 7 V, and devices for some ECL gates can break down at even lower voltages.

10.5.1 Emitter-Base Breakdown Voltage

Emitter-base breakdown voltage is determined by the doping concentration and radius of curvature of the junction, as was discussed previously in Section 9.1.2. Breakdown occurs first in the region of the junction where the electric field is the largest, usually corresponding to the portion of the junction where the doping levels are the highest. The actual breakdown voltage is then determined by the doping on the more lightly doped side of the junction.

In order to achieve high current gain, the emitter region is doped heavily, and the breakdown voltage of this junction will be determined by the impurity concentration of the more lightly doped base region. The base impurity concentration is highest at the surface, so the emitter-base junction will tend to break down first at the surface. The curvature of the junction enhances the electric field and reduces the breakdown voltage. Figure 10.5 gives the breakdown voltage of the emitter-base junction as a function of the final surface concentration of the base region, with junction radius as a parameter. Emitter-base breakdown voltages are low because of the relatively large impurity concentrations on both sides of the junction.

Example 10.4: An *npn* transistor has a 1-μm-deep emitter-base junction and the base diffusion given in Example 4.2. What is the expected breakdown voltage of this junction?

Solution: The base-region surface concentration in Fig. 4.9 is $1.1 \times 10^{18}/\text{cm}^3$. Figure 10.5 predicts the breakdown voltage of a 1-μm-deep junction with this surface

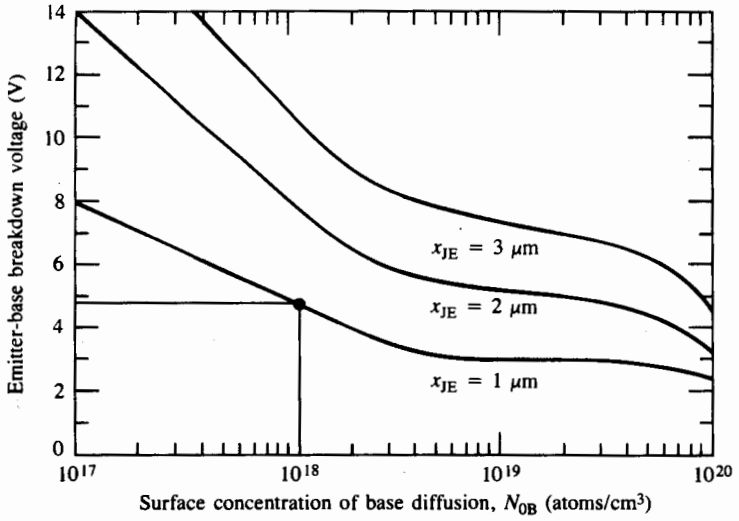


Fig. 10.5 Emitter-base junction breakdown voltage as a function of base surface concentration with emitter-base junction depth as a parameter. After ref. [4]. Reprinted with permission from *Solid-State Electronics,* Vol. 17, P. R. Wilson, "The Emitter-Base Breakdown Voltage of Planar Transistors," Copyright 1974, Pergamon Press, Ltd.[3]

concentration to be approximately 4.8 V. (The emitter-base junction of most common bipolar transistors will break down well below 10 V.)

10.5.2 Collector-Base Breakdown Voltage

The bipolar transistor can begin to conduct excessive collector current by two mechanisms. The first is Zener or avalanche breakdown of the collector-base junction. As discussed above, breakdown is localized to the region where the doping concentrations are the largest, but it is determined primarily by the doping concentration on the more lightly doped side of the junction. The collector is formed in the uniformly doped epitaxial layer. The base region is diffused into the epitaxial layer and is the more heavily doped side of the junction. Since the collector is uniform, junction breakdown will occur first where the electric field is enhanced by junction curvature. The breakdown voltage for the collector-base junction as a function of epitaxial-layer impurity concentration and junction radius is given in Fig. 10.6.

The second breakdown mechanism is punch-through of the base region, illustrated in Fig. 10.7. The epitaxial layer is more lightly doped than the base region, and the collector-base junction depletion layer extends predominantly into the epitaxial layer. As the collector-base voltage increases, the depletion layer expands further into the epitaxial

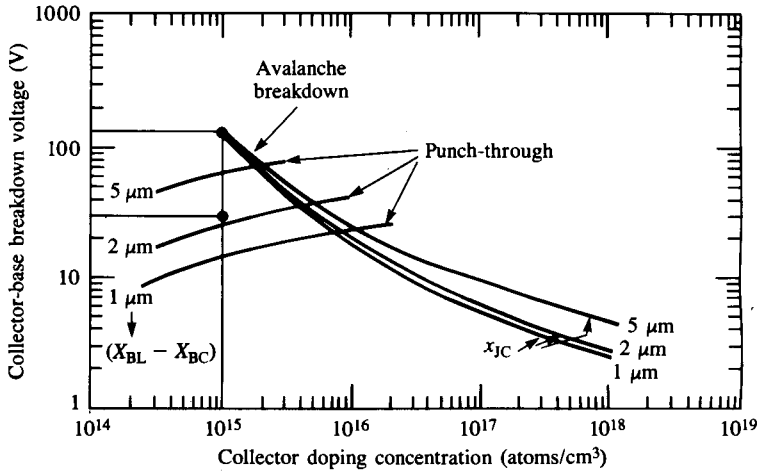


Fig. 10.6 Collector-base junction breakdown voltage as a function of collector-doping concentration with collector-base junction depth and punch-through limits as parameters. After ref. [4]. Reprinted from the JOURNAL OF THE ELECTROCHEMICAL SOCIETY, Volume 113 (1966), pages 508–510, by permission of the publisher, The Electrochemical Society, Inc.,[11] and Pergamon Press, Ltd.[12]

layer and will eventually hit the n^+ buried layer. At this point, further depletion-layer expansion will occur in the base, and any increase in collector-base voltage will quickly punch through the remaining base region.

The second set of curves in Fig. 10.6 shows collector-base junction breakdown limitations set by punch-through. As described above, the primary parameters determining the punch-through voltage are the epitaxial-layer doping and the width, $X_{BL} - X_{BC}$, of the region between the collector-base junction and the n^+ buried layer.

Example 10.5: What is the collector-base breakdown voltage of a transistor with a 10-μm-thick epitaxial layer doped at a level of 10^{15}/cm^3 if the collector-base junction depth is 5 μm? Assume that the buried layer has diffused upward 2 μm.

Solution: First, determine the avalanche breakdown voltage of an isolated *pn* junction. Figure 10.6 gives a breakdown voltage of approximately 130 V for a doping of 10^{15}/cm^3. Next, we must also check the punch-through limitations for $X_{BL} - X_{BC} = 3$ μm. From Fig. 10.6, the transistor will punch through at approximately 30 V. So the collector-base breakdown voltage is limited to 30 V by punch-through in this transistor.

As usual, different device requirements produce conflicting design constraints. High Zener breakdown voltage requires low epitaxial-layer doping. Low epitaxial-layer doping requires a relatively wide epitaxial-layer thickness in order to prevent punch-through.

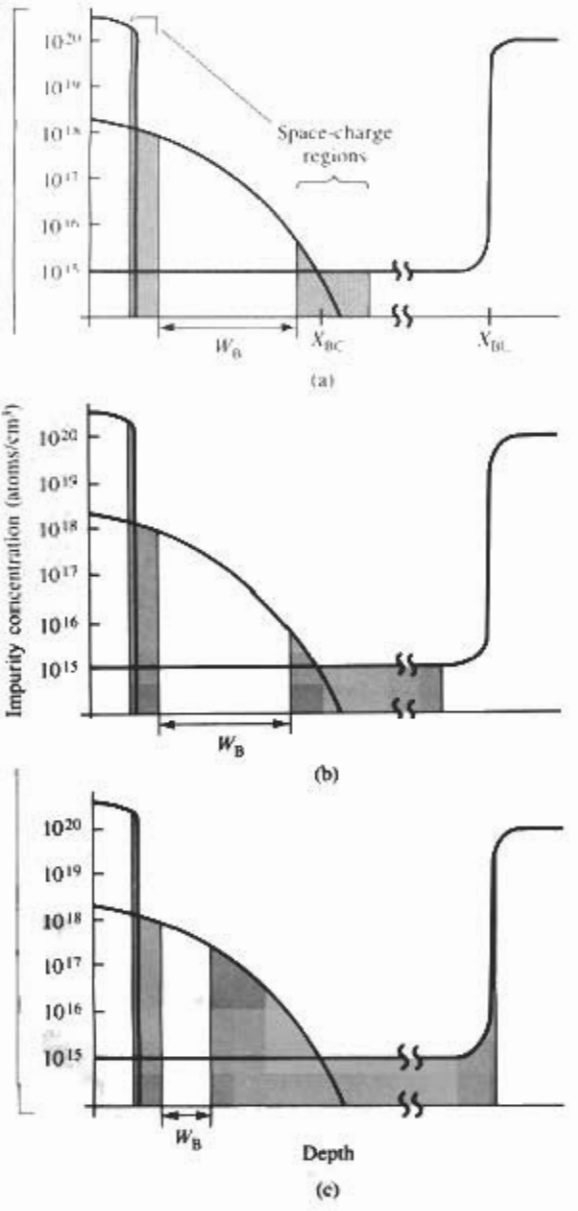


Fig. 10.7 Collector-base space-charge region growth as the collector-base voltage is increased. (a) Zero bias; (b) intermediate collector-base voltage; (c) large collector-base voltage just below the punch-through voltage.

However, a wide depletion-layer width in the epitaxial layer increases the transit time and reduces the frequency response of the device.

10.6 LAYOUT CONSIDERATIONS

This section will explore mask layout for the SBC transistor. The analysis will expand our understanding of the interaction of process design and layout. In particular, the top view of the mask set for a bipolar transistor often differs greatly from the final device structure due to large lateral diffusions, although this is less true of the high-performance digital technology to be discussed in Section 10.7.

10.6.1 Buried-Layer and Isolation Diffusions

The spacing between adjacent buried layers and the width of the intervening isolation diffusion determines how closely two transistors can be spaced. To maintain electrical isolation, the substrate is tied to the most negative voltage present in the circuit. The collector of a transistor, on the other hand, is often connected to the most positive voltage in the same circuit. Thus, the collector-substrate junction must be designed to support a voltage equal to the sum of the positive and negative voltages supplying the circuit. For analog circuits, this is typically more than 40 V. A typical design value of 60 V would provide an adequate safety margin.

Figure 10.8 shows the depletion layer in the p and n material near the isolation region of the transistor. The doping of the isolation diffusion is heavy at the surface and intersects the original substrate to produce isolation. At the surface, the window defining the isolation diffusion may be a minimum feature size, but the total width of the isolation region at the surface will be determined by lateral diffusion. For example, if the epitaxial layer is 15 μm thick and the minimum feature size is 10 μm, the isolation region will approach 40 μm in width, assuming lateral diffusion equals vertical diffusion.

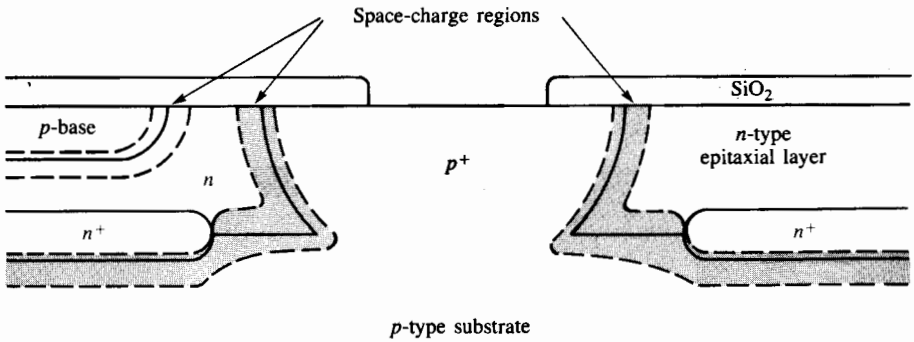


Fig. 10.8 Isolation region between two bipolar transistors. The spacing must be large enough to ensure that the two space-charge regions do not merge together.

The n^+ buried-layer diffusion is not usually permitted to intersect the p^+ isolation diffusion. If the two diffusions meet, the breakdown voltage of the junction will decrease, and the capacitance of the junction will increase. Thus, there will be a layout design rule associated with the minimum spacing between the n^+ region and the isolation diffusion.

10.6.2 Base Diffusion to Isolation Diffusion Spacing

At the surface, the collector-base and collector-substrate depletion regions of Fig. 10.8 must not merge. The minimum spacing can be determined from a knowledge of the applied voltages and the epitaxial-layer impurity concentration. Additional spacing must be added to account for the alignment sequence and accumulated alignment tolerances.

Example 10.6: What is the minimum spacing between the edge of the base diffusion and the edge of the isolation diffusion at the surface of a bipolar transistor if the alignment tolerance is 5 μm and the epitaxial-layer resistivity is 10 ohm-cm? Assume the two junctions must each support 40 V. Use a collector-base junction depth of 5 μm.

Solution: A 10-ohm-cm epitaxial layer has an impurity concentration of $5 \times 10^{14}/\text{cm}^3$, giving a value of $V/N_B = 8 \times 10^{-14}$ V-cm^3. From Fig. 10.6, the total depletion-layer width is approximately 10 μm, with 8.7 μm in the epitaxial layer. The conditions at the isolation-collector junction are essentially the same, so the minimum spacing will be two times the depletion-layer width of 8.7 μm plus the alignment tolerance of 5 μm for a total of 22.4 μm.

10.6.3 Emitter-Diffusion Design Rules

The minimum spacing between the edges of the emitter and base diffusions must be greater than the sum of the emitter and collector depletion-layer widths in the base, the accumulated alignment tolerance between the emitter and base masks, and the active base-region width.

In the basic SBC process, the n^+ emitter diffusion is also used to ensure formation of a good ohmic contact to the collector, and this collector contact diffusion should not intersect the depletion layers associated with either the p-type base or isolation diffusions. If this occurs, the breakdown voltage of the junctions will be reduced and the junction capacitances increased. (See Problem 10.7.)

10.6.4 A Layout Example

A set of design rules for a hypothetical bipolar transistor is given in Table 10.1, and Fig. 10.9 shows the layout of a minimum-size transistor based on these rules and making maximum use of lateral diffusion. It is interesting to note that the active area of the transistor, the region directly under the emitter, is a small fraction of the total device area

Table 10.1 Bipolar Transistor Design Rules for Fig. 10.9.

Minimum feature size	5 μm
Worst-case alignment tolerance between levels	2 μm
Epitaxial-layer thickness	10 μm
Collector-base junction depth	5 μm
Emitter-base junction depth	3 μm
Minimum emitter-to-collector spacing at surface	5 μm
Minimum base-to-isolation spacing at surface	5 μm
Minimum collector contact n^+ diffusion to isolation spacing	5 μm
Minimum collector contact n^+ diffusion to base spacing	5 μm
Buried-layer diffusion (both up and down)	2 μm
Buried layer to isolation spacing	5 μm
Lateral diffusion = vertical diffusion	

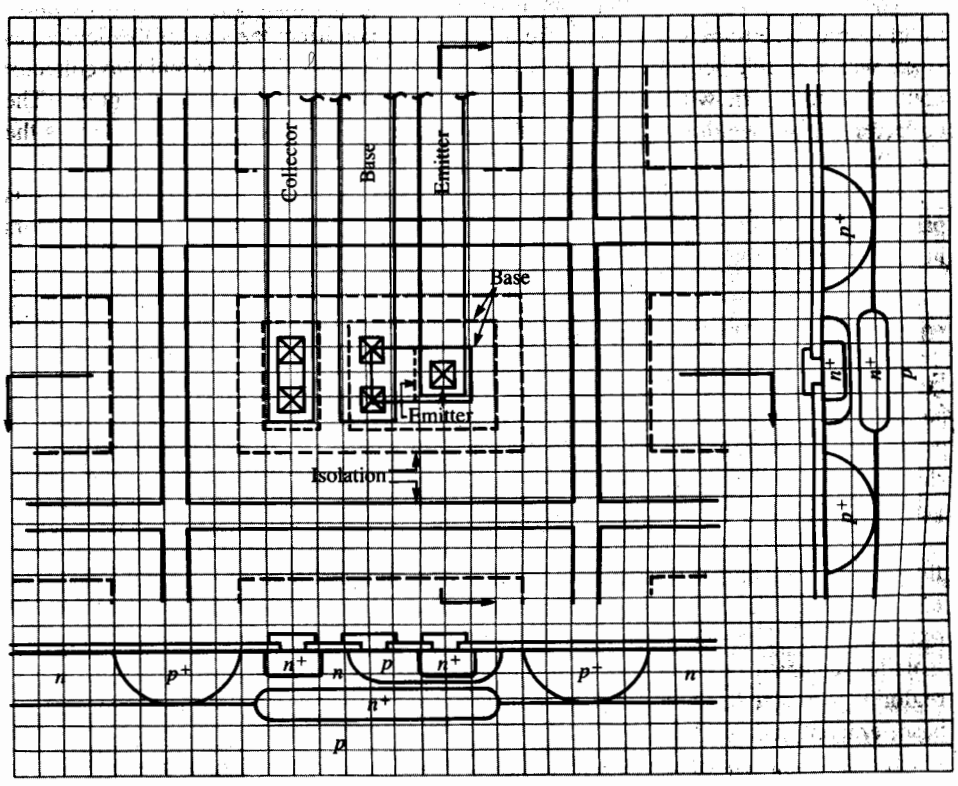


Fig. 10.9 Minimum-size bipolar transistor layout based on the design rules of Table 10.1. The buried layer is not shown in the top view for reasons of clarity.

of approximately 4536 μm^2. The final emitter area is 11 × 11 μm, or 121 μm^2, which represents only 2.67% of the total area of the transistor.

The rest of the area is needed to make contacts, to support depletion layers, and to provide isolation between adjacent devices. In this layout, the isolation area is 2800 μm^2, or more than 60% of the total area! Minimization of the isolation region represents an important issue in high-performance devices, not only for density improvement but also for junction-capacitance reduction.

The solid lines in the top view of the transistor layout represent the edges of the masks used to fabricate the transistor. The various dotted lines represent the final positions of the emitter, base, and isolation diffusions. For the design rules of Table 10.1, the window for the emitter diffusion happens to coincide exactly with the emitter contact window. The lateral diffusion of 3 μm provides more than the required 2-μm alignment tolerance for the emitter contact window.

The base diffusion is 5 μm deep and is assumed to diffuse laterally 5 μm. In the layout, the base contact windows actually extend outside the base region at the mask level but are more than one alignment tolerance within the base region following diffusion. This is an excellent example of the interaction between processing and layout.

The width of the base-contact metallization has been widened to more than a minimum feature size to help clarify the figure. This did not affect the size of the device, as space was available because of other design rule limitations. Two base and two collector contact windows fit within the minimum base and n^+ collector contact regions. The collector contact windows align with the edges of the n^+ diffusion window, as was the case for the emitter.

The buried-layer mask has also been omitted from the figure for clarity. In this particular structure, the design rules relating to the buried layer are not limiting factors in the size of this layout.

10.7 ADVANCED BIPOLAR STRUCTURES

For digital logic circuits, structures are optimized to provide as short a transit time as possible. This requires minimizing the basewidth, eliminating as much capacitance as possible by minimizing total junction area, minimizing the width of the collector space-charge region, and reducing the collector and base series resistances. A reduced current gain is traded for a shorter transit time.

Figure 10.10 shows a high-performance bipolar structure which attempts to achieve these goals by using a very thin epitaxial layer and shallow ion-implanted base and emitter regions. As much *pn* junction area as possible is eliminated through the use of oxide isolation. The sides of the emitter and base regions are actually walled by the oxide isolation regions. The n^+ buried layer is relatively large to minimize r_C, and the total base region is minimized to reduce the base resistance. Self-aligned contacts are made to the base, emitter, and collector regions.

The formation of the transistor of Fig. 10.10 begins with implantation and diffusion of the buried layer with a typical sheet resistance of 10 to 50 ohms per square. The

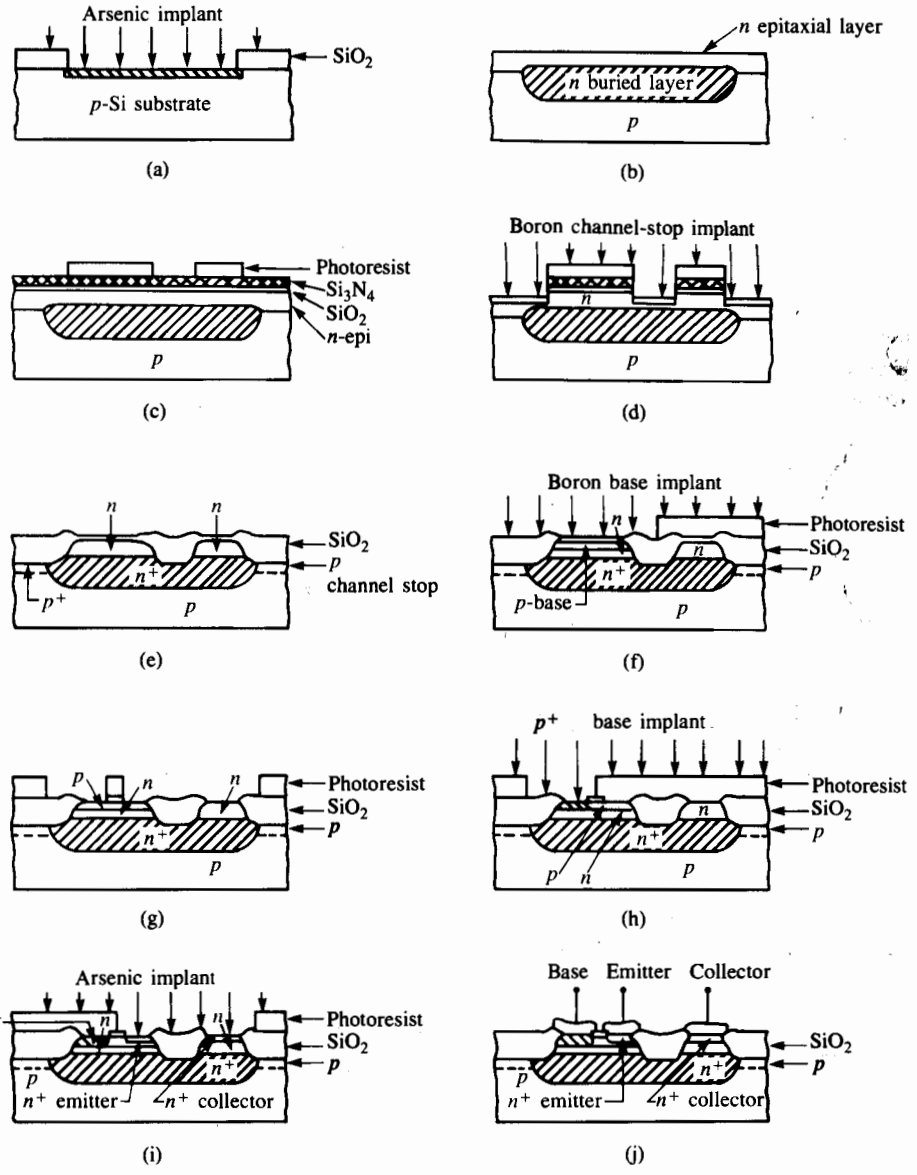


Fig. 10.10 Process sequence for a high-performance oxide-isolated bipolar transistor. (a) Buried-layer formation; (b) epitaxial layer growth; (c) mask for selective oxidation; (d) boron implant prior to recessed oxide growth; (e) selective oxidation; (f) base mask and boron base implantation; (g) emitter, base contact, and collector contact mask; (h) p^+ base contact implantation; (i) arsenic implantation for emitter and collector contact; (j) structure completed with multilayer metallization.

masking oxide is removed, and a thin epitaxial layer is grown on the surface. A recessed oxide isolation process is used to form the isolation regions between devices and to eliminate unnecessary junction area between the collector and emitter contacts. Prior to oxidation, part of the epitaxial layer is etched away so that the subsequent oxidation will extend completely through the epitaxial layer. An implantation is used to overcome boron depletion in the substrate during oxidation.

Next, the silicon nitride–oxide sandwich is removed, and an oxide is regrown on the surface. A boron implantation creates the shallow active base region. A mask is used to create windows for the emitter, and contacts to the base, emitter, and collector are all defined at the same time. Note that a single oxide strip defines both the emitter and base contact regions, eliminating alignment tolerances that would be needed if the regions were formed separately. The width of this strip is set by the metal-to-metal spacing plus accumulated alignment tolerances.

Photoresist is used as a barrier material during implantation of the base contact region. This p^+ implantation further reduces the base resistance of the device. Photoresist is also used as a barrier material during implantation of the emitter and collector contact regions. Note that these two mask steps use noncritical *blockout* masks similar to those used for threshold adjustment in a CMOS process.

Contacts are made through the same openings used for the base and emitter implantations. These contact areas are all cleared by a short wet or dry etch prior to metallization. Because of the very shallow junction depths involved in this structure, the metallization will be a multilayer sandwich structure including a barrier metal in the contact region. Interconnection of devices to form circuits will typically involve a multilevel metal process.

Figure 10.11 shows another high-performance structure which uses deep-trench isolation. The trenches are formed using reactive-ion etching and are refilled with polysilicon and silicon dioxide. In this structure, the emitter, and the contacts to the base and collector, are all formed by impurity diffusion from doped polysilicon.[6]

10.8 OTHER BIPOLAR ISOLATION TECHNIQUES

Several other interesting approaches to device isolation have been developed over the years, and three are surveyed here. The dielectric isolation process is still in use in high-performance analog circuits; the others have been largely replaced by oxide-isolated structures.

10.8.1 Collector-Diffusion Isolation (CDI)

The collector-diffusion-isolation[7] structure, shown in Fig. 10.12, was developed primarily for digital applications. The process eliminates the p-type isolation diffusion, achieving reduced device area and process complexity.

The process starts with diffusion of a low-sheet-resistance buried layer which will serve as the collector of the transistor. A thin p-type epitaxial layer forms the base region

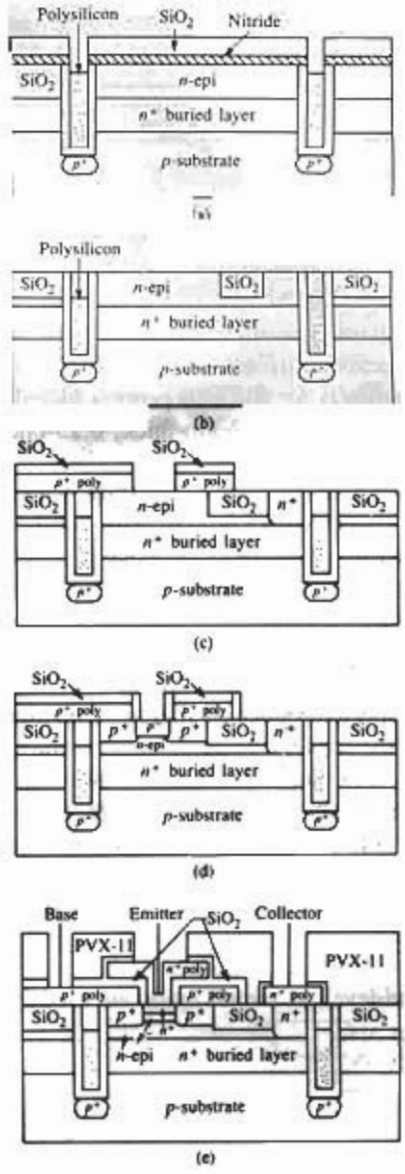


Fig. 10.11 A high-performance bipolar transistor structure with an f_T of 10 GHz. (a) Isolation is achieved using deep-trench isolation with polysilicon and silicon dioxide refill; (b) structure following selective oxidation; (c) p^+ polysilicon deposited and patterned; (d) diffusion from doped polysilicon forms the extrinsic base region and base contacts; a self-aligned implantation forms the intrinsic base; (e) diffusion from n^+ polysilicon forms the emitter and the emitter and collector contacts of the transistor. Copyright 1985 IEEE. Reprinted with permission from ref. [6].

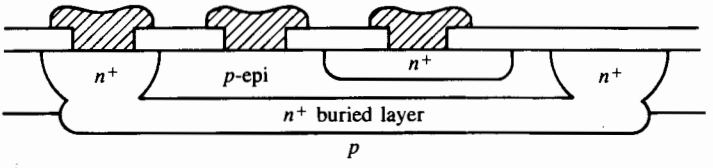


Fig. 10.12 Cross section of a transistor fabricated in the CDI process.[7]

and is grown in the next step. Device isolation is achieved via an n^+ diffusion which completely encloses the transistor and also provides the collector contact area. A shallow emitter is next implanted and/or diffused into the device, followed by contacts and metallization. Typical parameters for the CDI process include a buried-layer sheet resistance of 15 to 30 ohms per square, a 2-μm-thick, 0.25-ohm-cm epitaxial layer, and an emitter depth of less than 1 μm.

This process can produce high-performance, narrow-base transistors with minimum r_C but with relatively large collector-base and collector-substrate capacitances. It has for the most part been replaced with advanced oxide isolated structures which also minimize these capacitances, although at a cost of considerable process complexity.

10.8.2 V-Groove Isolation

V-groove isolation[8–9] attempts to produce small-geometry, high-frequency, bipolar transistors by eliminating the capacitance of junction isolation, as shown in Fig. 10.13. Anisotropic etching produces V-grooves which separate the transistors. ⟨100⟩ silicon must be used in this process to permit formation of the grooves.

The process looks very similar to the SBC process through diffusion of the p-type base region into the n-type epitaxial layer. The V-grooves are etched completely through the epitaxial layer, thereby achieving device isolation. An oxide-nitride sandwich is used to passivate the surface of the structure prior to formation of the n^+ emitter and collector contact regions. For shallow structures, a multilayer metallurgy is used to make contacts to the transistor, and several levels of metallization are used for circuit interconnection.

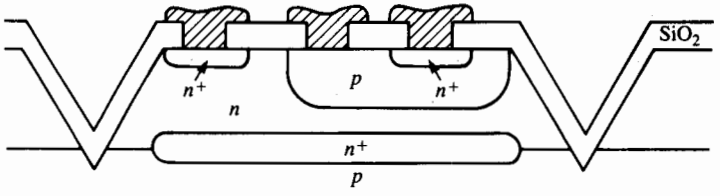


Fig. 10.13 A bipolar transistor formed using V-groove isolation.[8–9]

10.8.3 Dielectric Isolation

Figure 10.14 shows the steps used to achieve dielectrically isolated bipolar transistors.[10] Deep V-grooves are etched in the surface of ⟨100⟩-oriented silicon. A nonselective n^+ diffusion is performed, and a silicon dioxide layer is grown on the surface. A thick layer of polycrystalline silicon is then deposited on the surface of the wafer. Silicon is removed from the back surface of the wafer by lapping until the silicon dioxide in the V-grooves is exposed, as indicated by the dotted line in Fig. 10.14b. The surface is then mechanically and chemically polished. The wafer is turned over, yielding islands of silicon which are completely isolated from each other by the silicon dioxide dielectric layer. Standard processing is then used to form bipolar transistors.

This process is expensive, but an important variation permits formation of complementary, vertical *npn* and *pnp* transistors. It is used in fabrication of high-performance analog circuits. In addition, the structures are very tolerant to radiation and so are used in military applications.

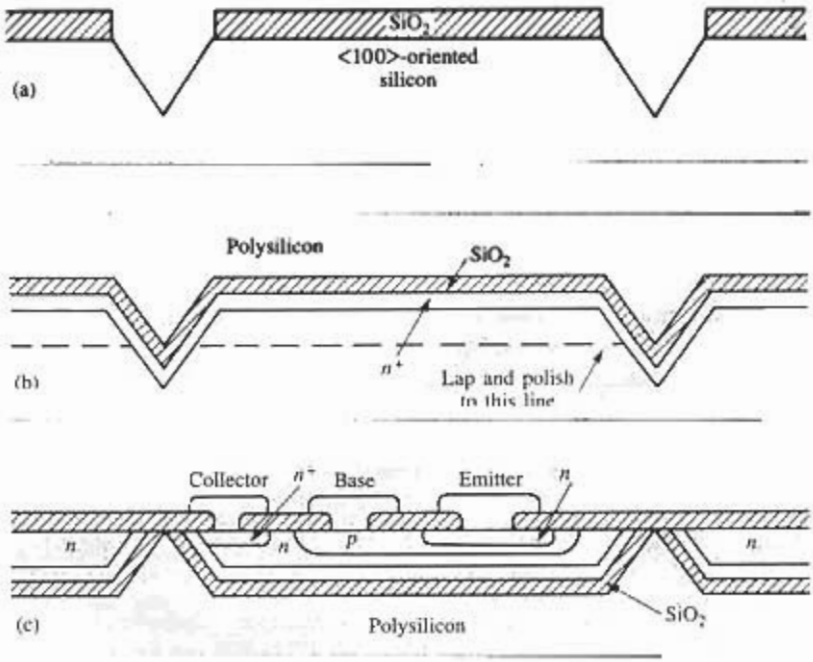


Fig. 10.14 Several steps in the dielectric isolation process.[10] (a) V-grooves anisotropically etched in the silicon substrate; (b) the structure following n^+ diffusion and oxidation; the wafer is turned over and lapped back and polished to the dotted line; (c) bipolar transistors are then fabricated in the isolated islands of silicon.

10.9 SUMMARY

The *standard buried collector* (SBC) process is widely used throughout the IC industry for analog and power circuit applications. More recently developed digital bipolar technologies have benefited greatly from process advances originally developed for use in MOS dynamic RAMs. These include oxide isolation, the use of polysilicon, and the introduction of ion implantation.

Bipolar technologies for analog applications are typically designed to yield current gains of several hundred with breakdown voltages of up to 50 V. The resulting devices have cutoff frequencies of less than 500 MHz. Devices for digital applications can operate with much lower current gains and supply voltages. These factors permit device designs with cutoff frequencies exceeding 5 GHz.

Collector-diffusion isolation, V-groove isolation, and dielectric isolation have all been developed as alternatives to the junction-isolated SBC process. These processes demonstrate the freedom that the process designer has in trying to achieve new and improved isolation techniques. However, the SBC process and oxide-isolated bipolar process remain the dominant technologies for today's analog and digital bipolar applications, respectively.

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PROBLEMS

10.1 Evaluate the Gummel number expressions for a uniformly doped transistor with impurity concentrations of N_E and N_B in the emitter and base, respectively. The effective width of the emitter is L_E, and W_B is the basewidth. Compare your result with eq. (2.46) in Volume III of this Series. What is the current gain for a device with $N_E = 10^{20}/cm^3$, $N_B = 10^{18}/cm^3$, $W_B = 4\ \mu m$, $L_E = 20\ \mu m$, $L_B = 50\ \mu m$, $D_B = 20\ cm^2/sec$, and $D_E = 5\ cm^2/sec$?

10.2 Using eq. (10.1), estimate the current gain of the transistor with the impurity profiles given in Fig. 10.2. Assume $W_B \ll L_B$, and $D_B = 20\ cm^2/sec$. Use $N_E/D_E = 5 \times 10^{13}\ sec/cm^4$, $x_{JE} = 1.5\ \mu m$, $x_{JC} = 4\ \mu m$.

10.3 What is the maximum collector-base breakdown voltage of a transistor with $X_{BL} - X_{BC} = 5\ \mu m$? What range of epitaxial layer dopings may be used to achieve this breakdown voltage?

10.4 A Zener reference diode is often formed using breakdown of the emitter-base junction.

(a) What base surface concentration is required to produce a breakdown voltage of 6 V for a 1-μm-deep junction?

(b) If the base surface concentration is too small by a factor of two, what is the actual breakdown voltage of the diode?

10.5 Calculate the collector-base depletion-layer width for the transistor of Example 10.3 using the expression for a one-sided step junction given in eq. (9.3). How does this compare with the width derived from Fig. 10.4?

10.6 The effective Gummel number in the emitter is substantially reduced from that calculated from the profile by bandgap narrowing in the emitter. Calculate N_E using the expressions in Chapter 4 for an As emitter with a sheet resistance of 10 ohms per square. Estimate D_E and compare N_E/D_E to the values stated in the text.

10.7 In Section 10.6.3 the importance of correct positioning of the n^+ collector contact diffusion was discussed. To illustrate this point, three simple *npn* transistors are fabricated in an *n*-type substrate using the structure drawn in Fig. P10.7. An n^+ collector ring is used to reduce the collector series resistance R_C. Three different spacings, 0 μm, 3 μm, and 5 μm, are used between the edge of the n^+ ring and the edge of the base diffusion. Explain why the breakdown voltage will be different for these three cases, and estimate the collector-base breakdown voltage for the three devices. Assume a base surface concentration of $10^{18}/cm^3$ and a junction depth of 5 μm.

10.8 Surface conditions can degrade the breakdown voltage of Zener diodes. Subsurface breakdown can be achieved using an ion-implanted process with the profile shown in Fig. P10.8. Estimate the breakdown voltage of this diode from Fig. 10.5.

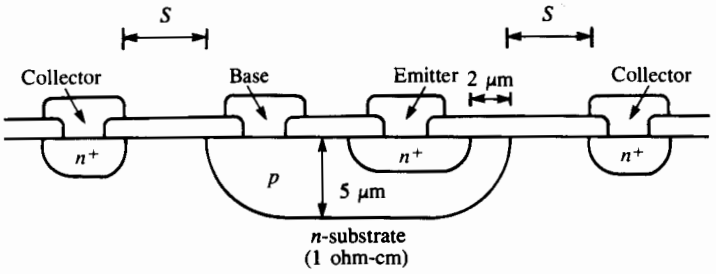

Fig. P10.7

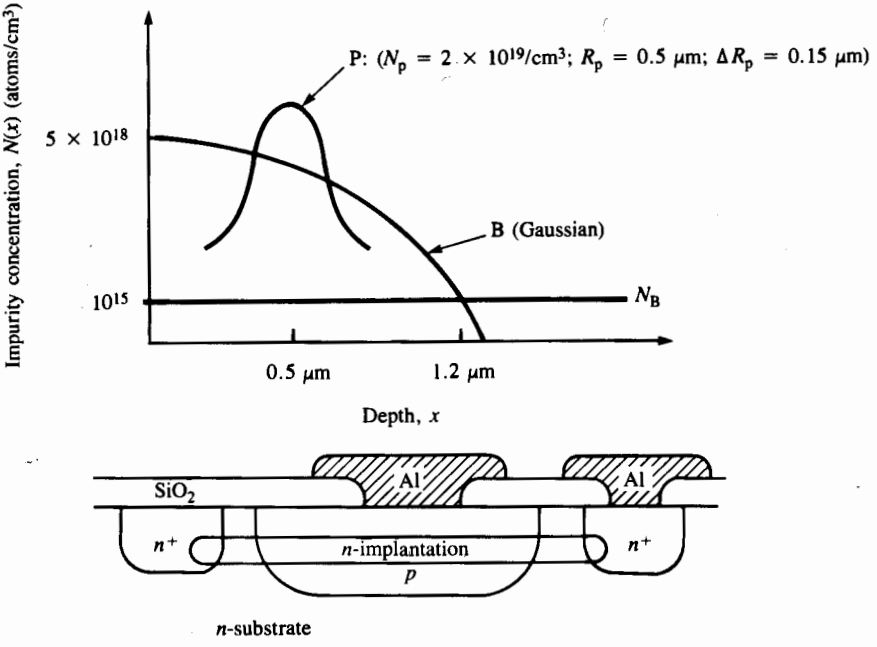

Fig. P10.8

10.9 A simple lateral *pnp* structure is shown in Fig. P10.9. The current gain of this transistor is collection-limited and does not obey eq. (10.1). Assume that the emitter injects current uniformly in all directions and that the collector collects all the current coming its way.

(a) Under these assumptions, what is the value of the common base current gain $\alpha = I_C/I_E$? What is the common emitter current gain β?

(b) Derive an expression for β as a function of the length and width of the device. For a given area, what relationship between the length and width maximizes the gain?

(c) What geometry would be used to optimize the current gain?

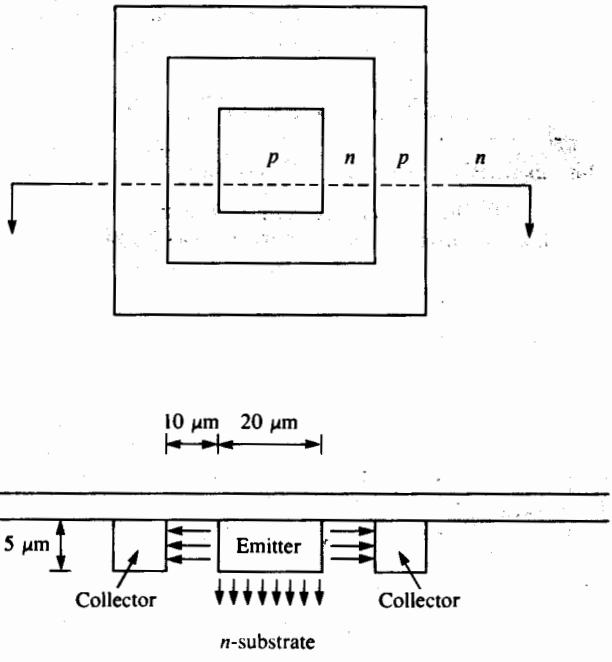

Fig. P10.9

10.10 It was noted that the CDI process is used mainly for digital applications. What characteristics of the structure make this true?

10.11 (a) How many masks are required for the CDI process?

(b) Design a good mask-alignment sequence for this process.

10.12 List the mask steps required for the oxide-isolated bipolar transistor of Fig. 10.11. Which are noncritical alignment steps?

10.13 Determine a reasonable diffusion schedule for the isolation diffusion of a junction-isolated structure with a 15-μm-thick epitaxial layer with the geometry of Fig. P10.13.

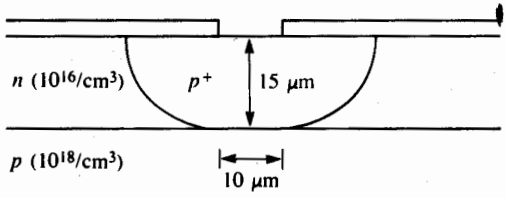

Fig. P10.13

(a) Assume that the width of the isolation at the bottom is to be 10 μm, that there is no up-diffusion from substrate, and that lateral diffusion equals vertical diffusion.

(b) Modify your diffusion time in part (a) to account for up-diffusion of boron from the substrate. Assume that the substrate represents an infinite supply of boron impurities with a constant concentration of $10^{18}/cm^3$.

10.14 The distance $X_{BL} - X_{BC} = 5\ \mu m$ in a certain bipolar SBC process with an epitaxial layer doping of $10^{15}/cm^3$. Use the one-sided step-junction formula, eq. (9.3), to estimate the punch-through voltage for this transistor. Compare with Fig. 10.6.

10.15 V-grooves in a ⟨100⟩ silicon make angles of 54.7° with the surface. What is the minimum isolation groove width at the surface if the epitaxial layer is 5 μm thick and we require a 1-μm minimum isolation width at the bottom of the groove? Does this seem competitive with other isolation processes? Which ones?

10.16 A CDI process uses a 0.25-ohm-cm epitaxial base layer and a 5-ohm-cm substrate. Estimate the breakdown voltages of the emitter-base and collector-base junctions. The emitter junction depth is 1 μm.