2 / Lithography

In order to produce an integrated circuit, thin films of various materials are used as barriers to the diffusion or implantation of impurity atoms, or as insulators between conductive materials and the silicon substrate. Holes or windows are cut through this barrier material wherever impurity penetration or contact is desired.

Masks contain the patterns of windows which are transferred to the surface of the silicon wafer using a process called *photolithography*. Photolithography makes use of a highly refined version of the photoengraving process. The patterns are first transferred from the mask to a light-sensitive material called *photoresist*. Chemical or plasma etching is then used to transfer the pattern from the photoresist to the barrier material on the surface of the wafer. Each mask step requires successful completion of numerous processing steps, and the complexity of an integrated-circuit process is often measured by the number of photographic masks used during fabrication. This chapter will explore the lithographic process, including mask fabrication, photoresist processes, and etching.

2.1 THE PHOTOLITHOGRAPHIC PROCESS

Photolithography encompasses all the steps involved in transferring a pattern from a mask to the surface of the silicon wafer. The various steps of the basic photolithographic process given in Figs. 2.1 and 2.2 will each be discussed in detail below.

Ultraclean conditions must be maintained during the lithography process. Any dust particles on the original substrate or that fall on the substrate during processing can result in defects in the final resist coating. Even if defects occur in only 10% of the chip sites at each mask step, less than 50% of the chips will be functional after a seven-mask process is completed. Vertical laminar-flow hoods in clean rooms are used to prevent particulate contamination throughout the fabrication process. Clean rooms use filtration to remove particles from the air and are rated by the maximum number of particles per cubic foot or cubic meter of air, as shown in Table 2.1. Clean rooms have evolved from the Class 10,000 to the Class 10 and even Class 1 facilities now being used for VLSI processing. For comparison, each cubic foot of ordinary room air has several million dust particles exceeding a size of 0.5 μm.

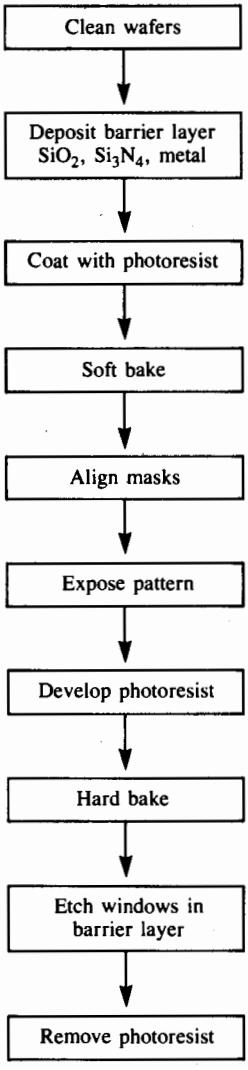


Fig. 2.1 Steps of the photolithographic process.

2.1.1 Wafer Cleaning

Prior to use, wafers are chemically cleaned to remove particulate matter on the surface as well as any traces of organic, ionic, and metallic impurities. A cleaning step in a solution of hydrofluoric acid is used to remove any oxide which may have formed on the wafer surface. A typical cleaning process is presented in Table 2.2.

One very important chemical used in wafer cleaning and throughout microelectronic fabrication processes is deionized (DI) water. DI water is highly purified and filtered to

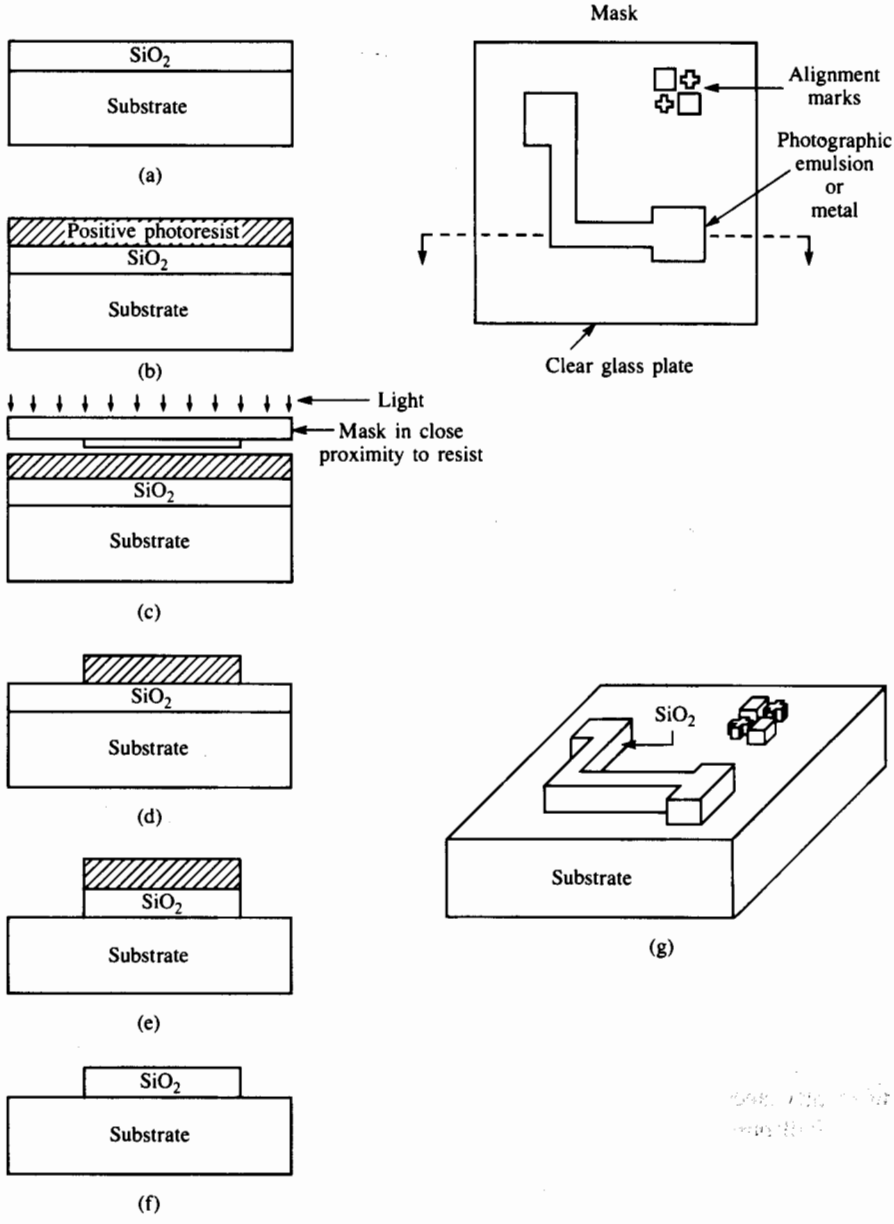


Fig. 2.2 Drawings of wafer through the various steps of the photolithographic process. (a) Substrate covered with silicon dioxide barrier layer; (b) positive photoresist applied to the surface of the wafer; (c) mask in close proximity to the surface of the resist-covered wafer; (d) substrate following resist exposure and development; (e) substrate following etching of the silicon dioxide layer; (f) oxide barrier on wafer surface after resist removal; (g) view of substrate with silicon dioxide pattern on the surface.

Table 2.1 Ratings by Class of Effectiveness of Filtration in Clean Rooms.

Class	Number of 0.5-μm particles per ft^3 (m^3)	Number of 5-μm particles per ft^3 (m^3)
10,000	10,000 (350,000)	65 (23,000)
1,000	1,000 (35,000)	6.5 (2,300)*
100	100 (3,500)	0.65 (230)*
10	10 (350)	0.065 (23)*
1	1 (35)*	0.0065 (2.3)*

*It is very difficult to measure particulate counts below 10 per ft^3.

Table 2.2 Silicon Wafer Cleaning Procedure.[4,5]

A. Solvent Removal
   1. Immerse in boiling trichloroethylene (TCE) for 3 min.
   2. Immerse in boiling acetone for 3 min.
   3. Immerse in boiling methyl alcohol for 3 min.
   4. Wash in DI water for 3 min.

B. Removal of Residual Organic/Ionic Contamination
   1. Immerse in a (5:1:1) solution of H_2O–NH_4OH–H_2O_2; heat solution to 75–80 °C and hold for 10 min.
   2. Quench the solution under running DI water for 1 min.
   3. Wash in DI water for 5 min.

C. Hydrous Oxide Removal
   1. Immerse in a (1:50) solution of HF–H_2O for 15 sec.
   2. Wash in running DI water with agitation for 30 sec.

D. Heavy Metal Clean
   1. Immerse in a (6:1:1) solution of H_2O–HCl–H_2O_2 for 10 min at a temperature of 75–80 °C.
   2. Quench the solution under running DI water for 1 min.
   3. Wash in running DI water for 20 min.

remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water at 25 °C is 18.3 Mohm-cm. Typical DI water systems achieve resistivities of 18 Mohm-cm with fewer than 1.2 colonies of bacteria per milliliter and with no particles larger than 0.25 μm.

2.1.2 Barrier Layer Formation

After cleaning, the silicon wafer is covered with the material which will serve as a barrier layer. The most common material is silicon dioxide (SiO_2), so we will use it as an

example here. Silicon nitride (Si_3N_4), polysilicon, photoresist, and metals are also routinely used as barrier materials at different points in a given process flow. Later chapters will discuss thermal oxidation, chemical vapor deposition, sputtering, and vacuum evaporation processes, all of which are used to produce thin layers of these materials.

The original silicon wafer has a metallic gray appearance. Once a silicon dioxide layer is formed on the silicon wafer, the surface will have a color which depends on the SiO_2 thickness. The finished wafer will have regions with many different thicknesses. Each region will produce a different color, resulting in beautiful, multicolored IC images, photographs of which appear in many books and magazines.

2.1.3 Photoresist Application

After formation of the SiO_2 layer, the surface of the wafer is coated with a light-sensitive material called *photoresist*. The surface must be clean and dry to ensure good photoresist adhesion. Freshly oxidized wafers may be directly coated, but if the wafers have been stored, they should be carefully cleaned and dried prior to application of the resist. A liquid adhesion promoter is often applied just prior to resist application.

Photoresist is typically applied in liquid form. The wafer is held on a vacuum chuck and then spun at high speed for 30 to 60 sec to produce a thin uniform layer. Speeds of 1000 to 5000 rpm result in layers ranging from 2.5 to 0.5 μm, respectively. The actual thickness of the resist depends on its viscosity and is inversely proportional to the square root of the spinning speed.

2.1.4 Soft Baking

A drying step called *soft baking* or *prebaking* is used to improve adhesion and remove solvent from the photoresist. Times range from 10 to 30 min in an oven at 80 to 90 °C in an air or nitrogen atmosphere. The soft-baking process is specified on the resist manufacturer's data sheet and should be followed closely. After soft baking, the photoresist is ready for mask alignment and exposure.

2.1.5 Mask Alignment

A photomask, a square glass plate with a patterned emulsion or metal film on one side, is placed over the wafer. Each mask following the first must be carefully aligned to the previous pattern on the wafer. Much of the alignment has traditionally involved manual operation of alignment equipment. VLSI designs with minimum-size geometrical features measuring 1.25 μm (minimum linewidth or space) require an alignment tolerance of better than ± 0.25 μm. Computer-controlled alignment equipment has been developed to achieve this level of alignment precision.

With manual alignment equipment, the wafer is held on a vacuum chuck and carefully moved into position below the mask using an adjustable x-y stage. The mask is

spaced 25 to 125 μm above the surface of the wafer during alignment. If contact printing is being used, the mask is brought into contact with the wafer after alignment.

Alignment marks are introduced on each mask and transferred to the wafer as part of the integrated-circuit pattern. The marks are used to align each new mask level to one of the previous levels. A sample set of alignment marks is shown in Fig. 2.3. For certain mask levels, the cross on the mask is placed in a box on the wafer. For other mask levels, the box on the mask is placed over a cross on the wafer. The choice depends on the type of resist used during a given photolithographic step. Split-field optics are used to simultaneously align two well-separated areas of the wafer.

2.1.6 Photoresist Exposure and Development

Following alignment, the photoresist is exposed through the mask with high-intensity ultraviolet light. Resist is exposed wherever silicon dioxide is to be removed. The photoresist is developed with a process very similar to that used for developing ordinary photographic film, using a developer supplied by the photoresist manufacturer. Any resist which has been exposed to ultraviolet light is washed away, leaving bare silicon dioxide in the exposed areas of Fig. 2.2d. A photoresist acting in the manner just described is called a *positive resist,* and the mask contains a copy of the pattern which will remain on the surface of the wafer. Windows are opened wherever the exposing light passes through the mask.

Negative photoresists can also be used. A negative resist remains on the surface wherever it is exposed. Figure 2.4 shows simple examples of the patterns transferred to a silicon dioxide barrier layer using positive and negative photoresists with the same mask. Negative resists were widely used in early integrated-circuit processing. However, positive resist yields better process control in small-geometry structures and is now the main type of resist used in VLSI processes.

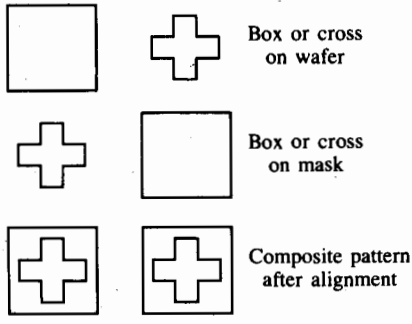


Fig. 2.3 A simple set of alignment marks. At some steps a cross may be aligned within a box. At others, a box may be placed around the cross. The choice depends on the type of resist being used at a given mask step.

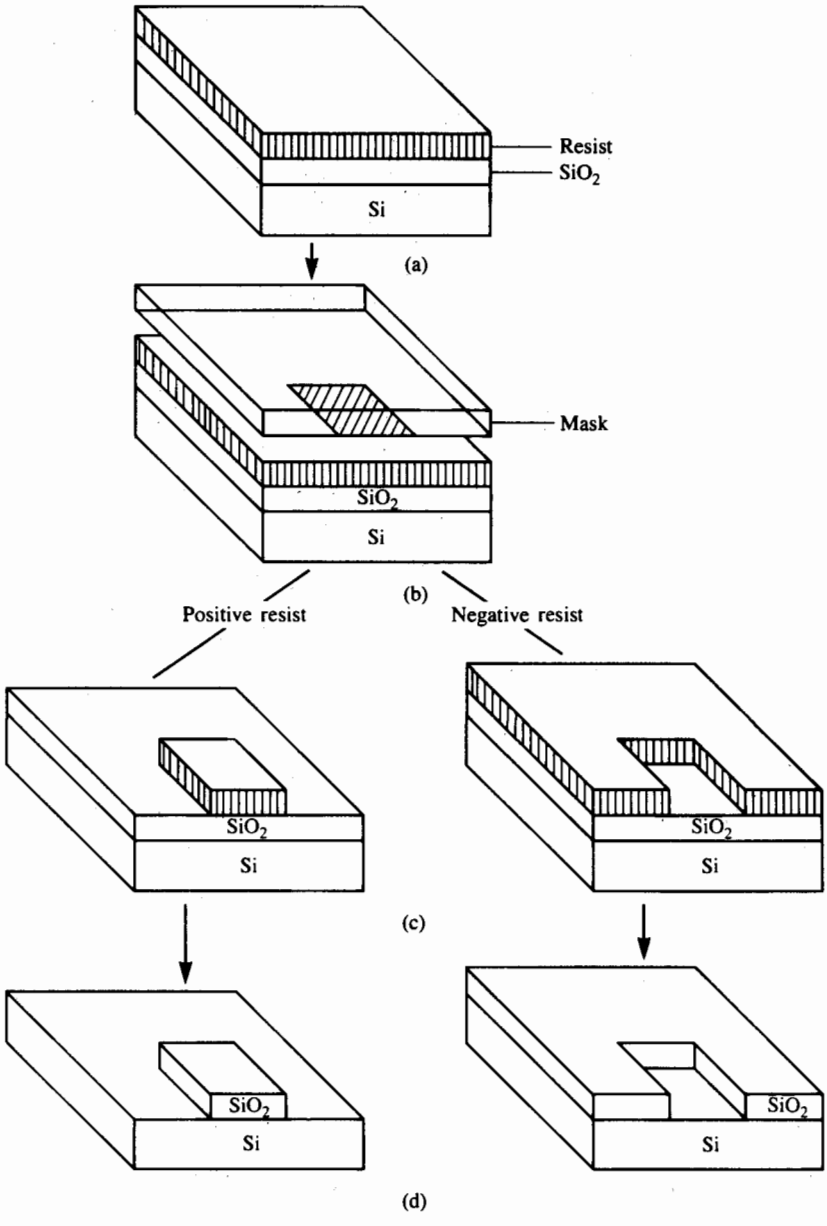


Fig. 2.4 Resist and silicon dioxide patterns following photolithography with positive and negative resists.

2.1.7 Hard Baking

Following exposure and development, a baking step is used to harden the photoresist and improve adhesion to the substrate. A typical process involves baking in an oven for 20 to 30 min at 120 to 180 °C. Details of this step are again specified on the manufacturer's photoresist data sheets.

2.2 ETCHING TECHNIQUES

Chemical etching in liquid or gaseous form is used to remove any barrier material not protected by hardened photoresist. The choice of chemicals depends on the material to be etched. A high degree of selectivity is required so that the etchant will remove the unprotected barrier layer much more rapidly than it attacks the photoresist layer.

2.2.1 Wet Chemical Etching

A buffered oxide etch (BOE or BHF) is commonly used to etch windows in silicon dioxide layers. BOE is a solution containing hydrofluoric acid (HF), and etching is performed by immersing the wafers in the solution. At room temperature, HF etches silicon dioxide much more rapidly than it etches photoresist or silicon. The etch rate in BOE ranges from 10 to 100 nm/min at 25 °C, depending on the density of the silicon dioxide film. Etch rate is temperature-dependent, and temperature is carefully monitored during the etch process. In addition, etch rates depend on the type of oxide present. Oxides grown in dry oxygen etch more slowly than those grown in the presence of water vapor. A high concentration of phosphorus in the oxide enhances the etch rate, whereas a reduced etch rate occurs when a high concentration of boron is present. High concentrations of these elements convert the SiO_2 layer to a phosphosilicate or borosilicate glass.

HF and water both wet silicon dioxide but do not wet silicon. The length of the etch process may be controlled by visually monitoring test wafers which are etched along with the actual integrated-circuit wafers. Occurrence of a hydrophobic condition on the control wafer signals completion of the etch step.

Wet chemical etching tends to be an isotropic process, etching equally in all directions. Figure 2.5a shows the result of isotropic etching of a narrow line in silicon

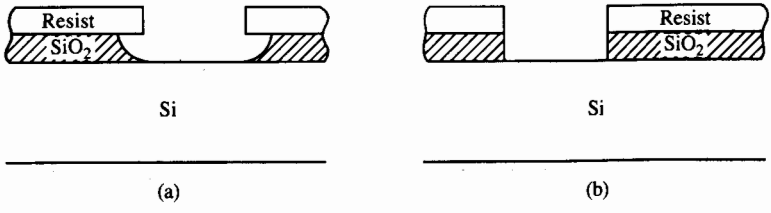


Fig. 2.5 Etching profiles obtained with (a) isotropic wet chemical etching and (b) dry anisotropic etching in a plasma or reactive-ion etching system.

dioxide. The etching process has etched under the resist by a distance equal to the thickness of the film. This "etch bias" becomes a serious problem in processes requiring linewidths with dimensions similar to the thickness of the film.

2.2.2 Dry Etching

Dry etching processes are widely used in VLSI fabrication. Highly anisotropic etching profiles can be obtained as shown in Fig. 2.5b, avoiding the undercutting problem of Fig. 2.5a characteristic of wet processes. Dry processes require only small amounts of reactant gases, whereas wet etching requires disposal of relatively large amounts of liquid chemical wastes.

Plasma etching immerses the wafers in a gaseous plasma created by RF excitation in a vacuum system. The plasma contains fluorine or chlorine ions which etch silicon dioxide. The RF power source typically operates at a frequency of 13.56 MHz, which is set aside by the Federal Communications Commission for industrial and scientific purposes.

Sputter etching uses energetic noble gas ions such as Ar^+ to bombard the wafer surface. Etching occurs by physically knocking atoms off the surface of the wafer. Highly anisotropic etching can be obtained, but selectivity is often poor. Metals can be used as barrier materials to protect the wafer from etching.

Reactive-ion etching combines the plasma and sputter etching processes. Plasma systems are used to ionize reactive gases, and the ions are accelerated to bombard the surface. Etching occurs through a combination of the chemical reaction and momentum transfer from the etching species.

2.2.3 Photoresist Removal

After windows are etched through the SiO_2 layer, the photoresist is stripped from the surface, leaving a window in the silicon dioxide. Photoresist removal typically uses proprietary-liquid resist strippers, which cause the resist to swell and lose adhesion to the substrate. Dry processing may also be used to remove resist by oxidizing (burning) it in an oxygen plasma system, a process often called *resist ashing*.

2.3 PHOTOMASK FABRICATION

Photomask fabrication involves a series of photographic processes outlined in Fig. 2.6. An integrated-circuit mask begins with a large-scale drawing of each mask. Early photomasks were cut by hand in a material called *rubylith*, a sandwich of a clear backing layer and a thin red layer of Mylar. The red layer was cut with a stylus and peeled off, leaving the desired pattern in red. The original rubylith copy of the mask was 100 to 1000 times larger than the final integrated circuit and was photographically reduced to form a reticle for use in a step-and-repeat camera, as described later

Today, computer graphics systems and optical pattern generators have largely supplanted the use of rubylith. An image of the desired mask is created on a computer

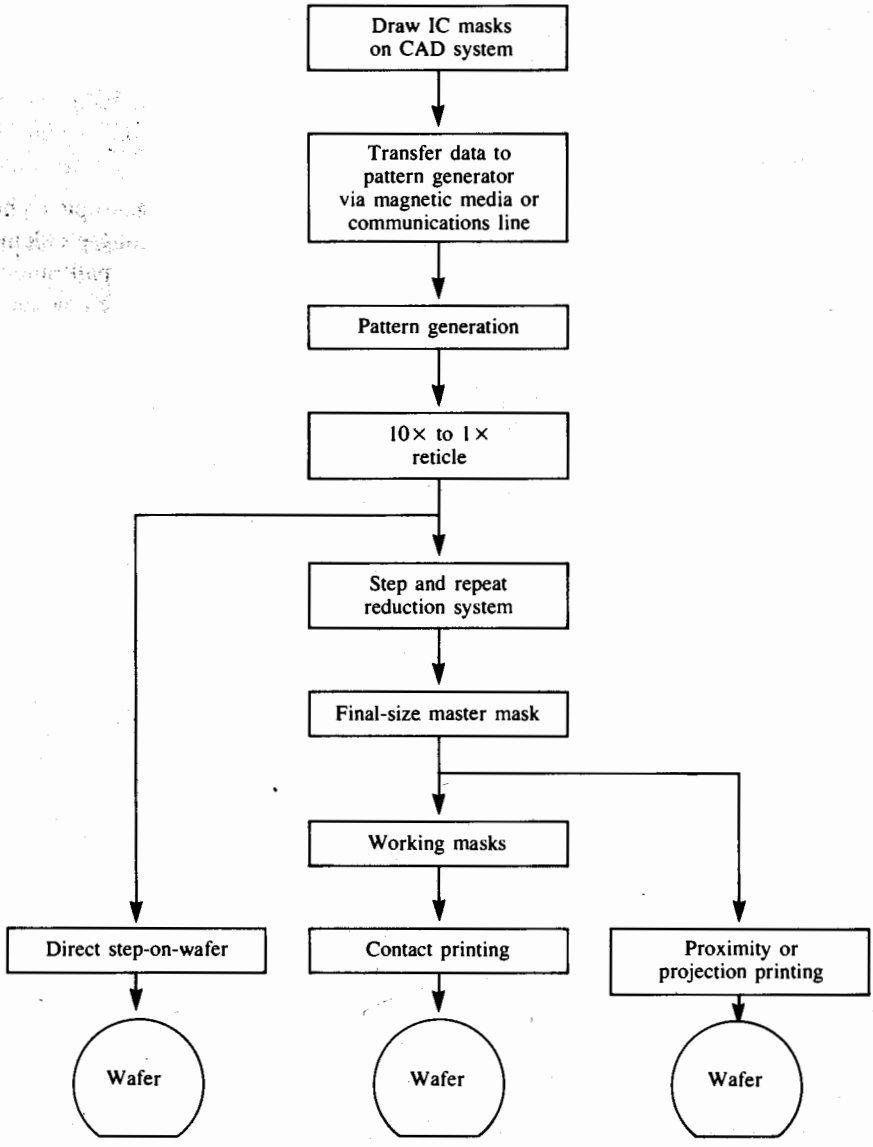


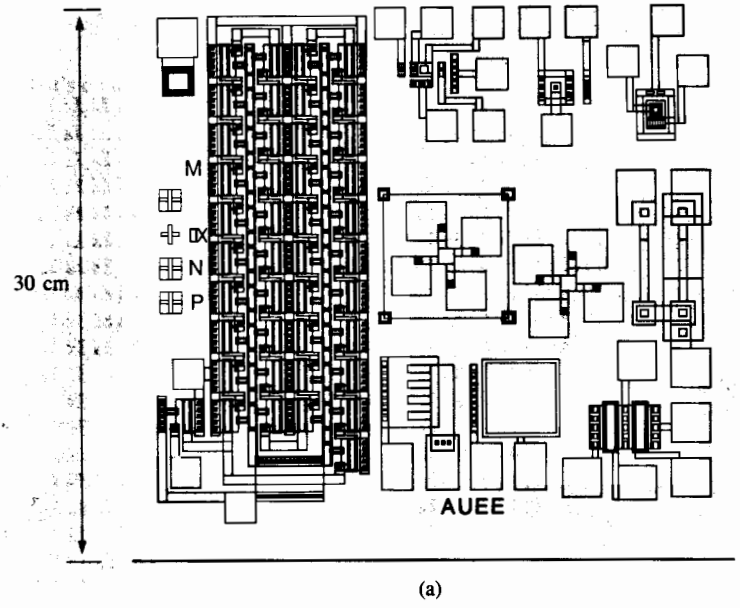
Fig. 2.6 Outline of steps in the mask fabrication process.

graphics system. Once the image is complete, files containing the commands needed to drive a pattern generator are created on magnetic tape or disks. The pattern generator uses a flash lamp to expose the series of rectangles composing the mask image directly onto a photographic plate called the *reticle*.

Reticle images range from one to ten times final size. A step-and-repeat camera is used to reduce the reticle image to its final size and to expose a two-dimensional array of images on a master copy of the final mask. On a 125-mm wafer, it is possible to get approximately 1900 copies of a 2.5 mm × 2.5 mm integrated-circuit chip! Figure 2.7 shows examples of a computer graphics plot, a reticle, and a final mask for a simple integrated circuit.

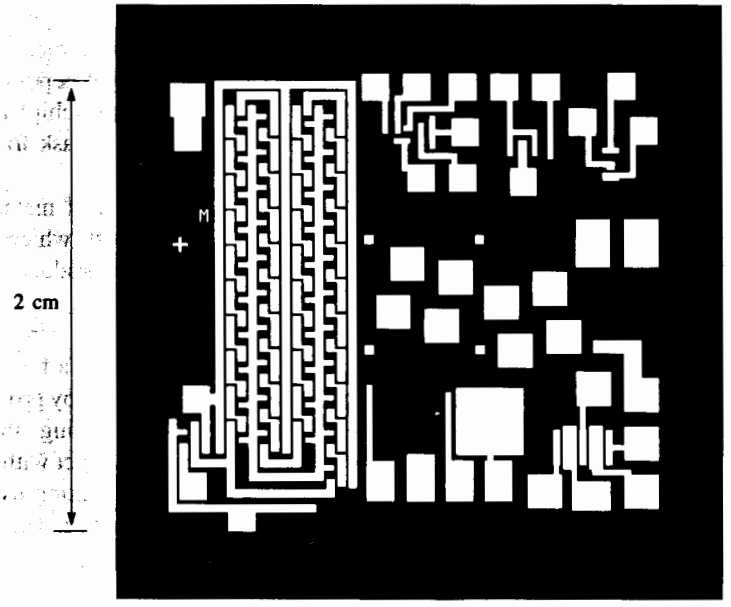
A final master copy of the mask is usually made in a thin film of metal, such as chrome, on a glass plate. The mask image is transferred to photoresist, which is used as an etch mask for the chrome. Working emulsion masks are then produced from the chrome master.

Each time a mask is brought into contact with the surface of the silicon wafer, the pattern can be damaged. Therefore, emulsion masks are used for only a few exposures before they are thrown away. Contact printing has been largely replaced by proximity and projection printing systems, illustrated in Fig. 2.8. In proximity printing, the mask is brought in very close proximity to the wafer but does not come in contact with the wafer during exposure, thus preventing damage to the mask. Projection printing uses a dual-lens system to project a portion of the mask image onto the wafer surface. The wafer and masks may be scanned or the system may operate in a step-and-repeat mode. The actual mask and lenses are mounted many centimeters from the wafer surface.

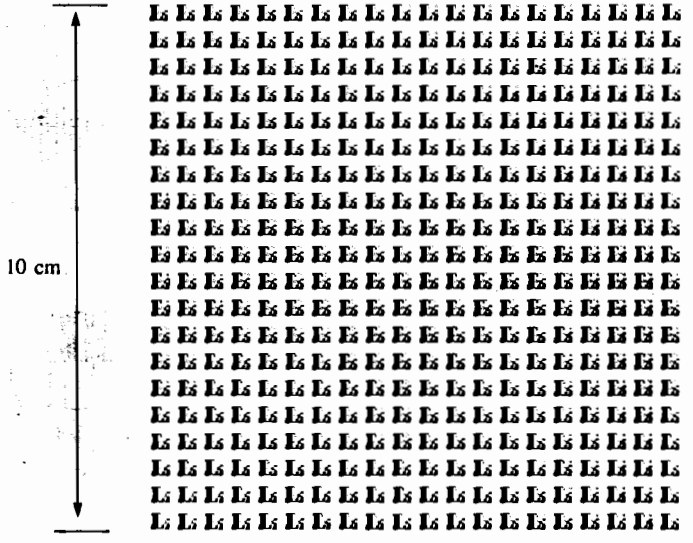


(a)

Fig. 2.7 Mask fabrication. (a) Composite computer graphics plot of all masks for a simple integrated circuit; (b) 10× reticle of metal-level mask; (c) final-size emulsion mask with 400 copies of the metal level of the integrated circuit in (a). (Figure continued on p. 24.)



(b)



(c)

Fig. 2.7 (continued)

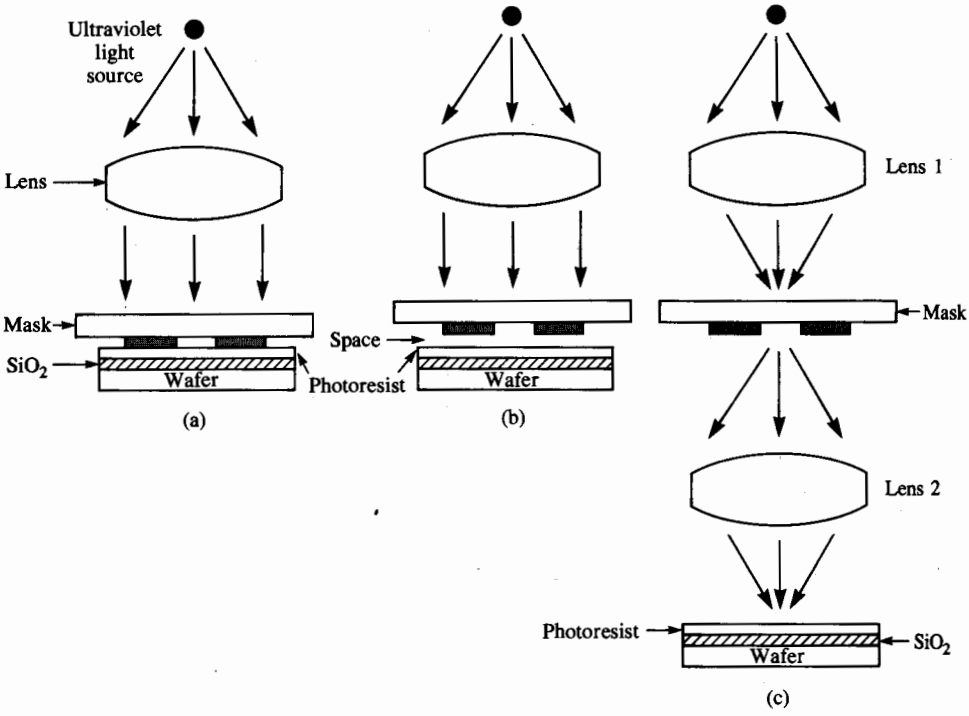


Fig. 2.8 Artist's conception of various printing techniques. (a) Contact printing, in which wafer is in intimate contact with mask; (b) proximity printing, in which wafer and mask are in close proximity; (c) projection printing, in which light source is scanned across the mask and focused on the wafer. Copyright, 1983, Bell Telephone Laboratories, Incorporated. Reprinted by permission from ref. [2].

In large-diameter wafers, it is difficult to maintain alignment between mask levels across the complete wafer, particularly with features whose size approaches 1 μm. High-resolution systems now use direct step-on-wafer techniques. A projection system is used with a 1× or 10× reticle to expose the integrated-circuit die pattern directly on the wafer. No step-and-repeat masks of the circuit are produced. The pattern is aligned and exposed separately at each die site.

Masks requiring geometrical features smaller than 1.25 μm can be produced by writing the pattern on the wafer in a special electron-sensitive resist using electron beams. Electron-beam systems are also commonly used to make 1× reticles for direct step-on-wafer systems.

2.4 SUMMARY

Photolithography is used to transfer patterns from masks to photoresist on the surface of silicon wafers. The resist protects portions of the surface while windows are etched in

barrier layers such as silicon dioxide, silicon nitride, or metal. The windows may be etched using either wet or dry processing techniques. Wet chemical etching tends to etch under the edge of the mask, causing a loss of linewidth control at small dimensions. Dry etching can yield highly anisotropic etching profiles and is required in most VLSI processing.

After etching, impurities can be introduced into the wafer through the windows using ion implantation and/or high-temperature diffusion, or metal can be deposited on the surface making contact with the silicon through the etched windows. Masking operations are performed over and over during integrated-circuit processing, and the number of mask steps required is used as a basic measure of process complexity.

Mask fabrication uses computer graphics systems to draw the chip image at 100 to 2000 times final size. Reticles one to ten times final size are made from this computer image, using optical pattern generators or electron-beam systems. Step-and-repeat cameras are used to fabricate final masks from the reticles, or direct step-on-wafer systems may be used to transfer the patterns directly to the wafer.

Today we are reaching the limits of optical lithography. Present equipment can define windows which are approximately 1.25 μm wide. (Just a few year ago, experts thought that 2 μm would be the limit! Today it appears that it may be possible to extend optical lithography to submicron dimensions.) The wavelength of light is too long to produce much smaller geometrical features because of fringing and interference effects. Electron-beam and X-ray lithography are now being used to fabricate devices with geometrical features smaller than 0.25 μm, and lithography test structures have reproduced shapes with minimum feature sizes of 0.1 μm.

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PROBLEMS

2.1 A complex CMOS fabrication process requires 15 masks. What fraction of the dice must be good (i.e., what yield must be obtained) during each mask step if we require 30% of the final dice to be good?

2.2 The mask set for a simple rectangular *pn* junction diode is shown in Fig. P2.2. The diode is formed in a *p*-type substrate. Draw a picture of the horizontal layout for the diode which results when a worst-case misalignment of 3 μm occurs in both the x and y directions on each mask level.

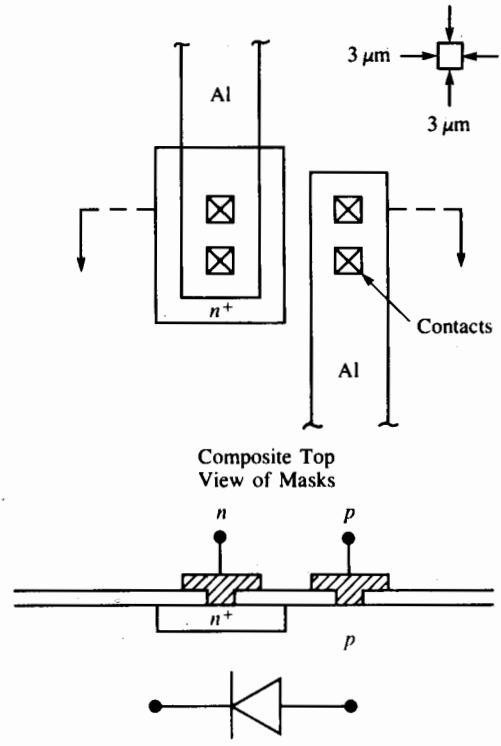

Fig. P2.2

(a) Assume that both the contact and metal levels are aligned to the diffusion level.

(b) Assume that the contact level is aligned to the diffusion level and the metal level is aligned to the contact level.

2.3 Figure P2.3 shows a resist pattern on top of a silicon dioxide film 1 μm thick. Draw the silicon–silicon dioxide structure after etching and removal of the photoresist for:

(a) Isotropic wet chemical etching

(b) Anisotropic dry etching with no undercutting.

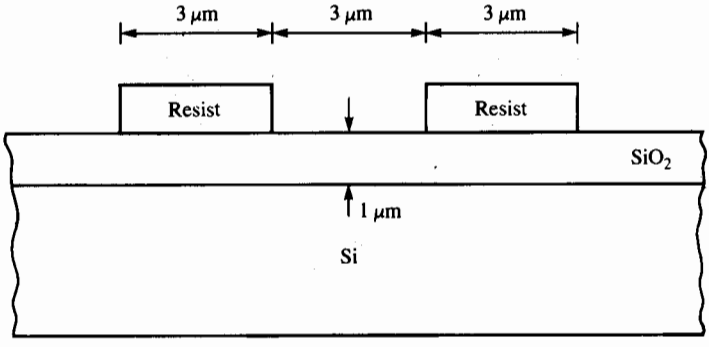

Fig. P2.3

2.4 (a) What type of photoresist must be used with each of the three mask levels (*n*-diffusion window, contact windows, and metal etch) used to fabricate the diode of Problem 2.2?

(b) Draw a set of alignment marks suitable for use with the alignment sequence of Problem 2.2b.