7 / Interconnections and Contacts

The previous six chapters have focused on the various processes used to fabricate semiconductor devices in the silicon substrate. To complete the formation of an integrated circuit, one must interconnect the devices and finally get connections to the world outside the silicon chip. Until the 1970s, integrated circuits had two possible levels of interconnection: diffusions and metallization. The use of polysilicon as a gate material in MOS devices added a third level useful for interconnecting devices and circuits.

In this chapter we discuss the various forms of interconnections and the problems associated with making good contacts between metal and silicon. Refractory metal silicides and multilevel metallization used in VLSI processes are discussed, and an additional method for depositing patterned films, called *liftoff*, is also introduced.

7.1 INTERCONNECTIONS IN INTEGRATED CIRCUITS

As we found in previous chapters, aluminum, polysilicon, and diffused regions are all easily isolated from each other using an insulating layer of silicon dioxide. Thus today's ICs have three different materials that may cross over each other. To be useful as an interconnect, the materials must also provide as low a sheet resistance as possible in order to minimize voltage drops along the interconnect lines as well as to minimize propagation delay caused by the resistance and capacitance of the line. Finally, low-resistance "ohmic" contacts must be made between the materials, and the interconnection lines must be reliable throughout long-term operation.

Figure 7.1 shows a simple MOS logic circuit which illustrates how polysilicon, aluminum, and diffused interconnections may cross over and/or contact each other. Aluminum is used to make contact to diffusions and polysilicon, and diffusions in various regions have been extended and merged together to form interconnections.

In this technology, polysilicon lines and diffused lines can only be connected together using the metal level. Improved circuit density can often be achieved by using "butted contacts" between polysilicon and diffusions or by changing the process to introduce "buried contacts" directly between the polysilicon and diffused layers. These two techniques will be examined later in this chapter.

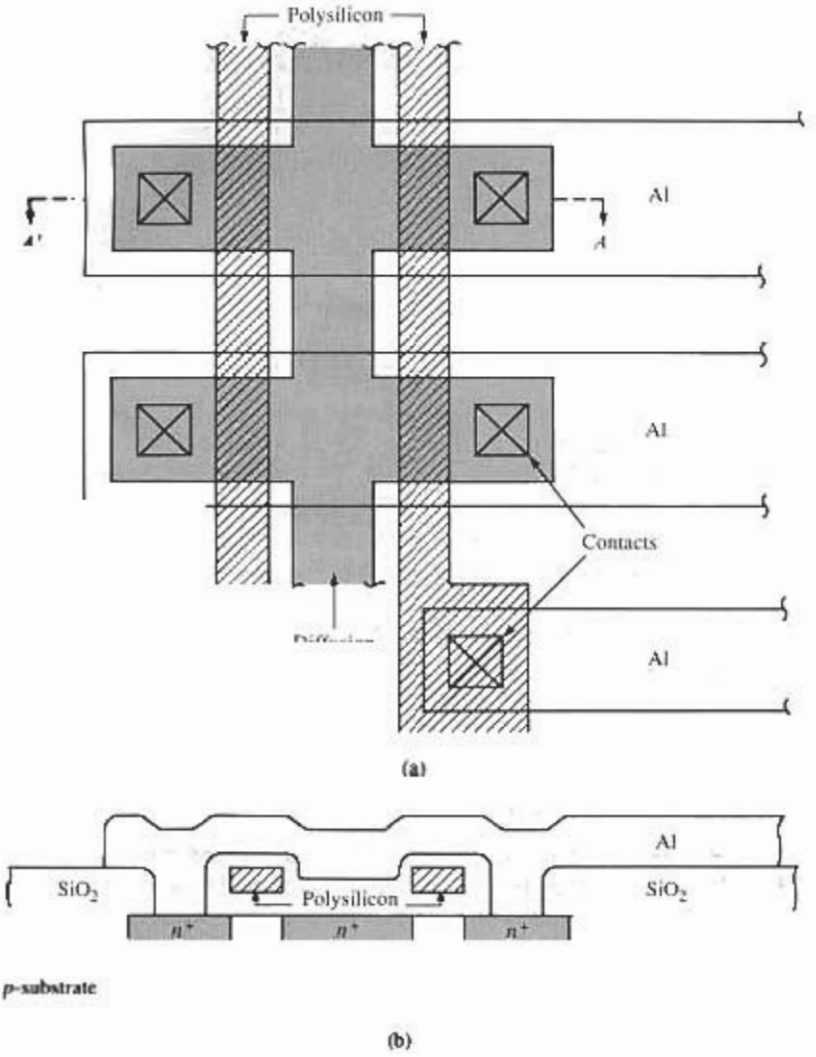

Fig. 7.1 Portion of a MOS logic circuit showing the use of diffusion, polysilicon, and aluminum interconnections. (a) Top view; (b) cross section through A'-A.

7.2 METAL INTERCONNECTIONS AND CONTACT TECHNOLOGY

The requirement for low-resistivity materials leads one to immediately consider metals for use as interconnections, and both aluminum and gold have been used with silicon IC processing. Gold requires the use of a multilayer metal sandwich involving other metals such as titanium or tungsten. In addition, gold can be troublesome because it is a very

rapid diffuser and produces deep-level recombination centers in silicon. Aluminum is compatible with silicon IC processing and is the most common material in use today. It is relatively inexpensive, adheres well to silicon dioxide, and has a bulk resistivity of 2.7 μohm-cm. However, care must be exercised to avoid a number of problems associated with the formation of good aluminum contacts to silicon.

7.2.1 Ohmic Contact Formation

We desire to form "ohmic" contacts between the metal and semiconductor. True ohmic contacts would exhibit a straight-line *I-V* characteristic with a low value of resistance (Fig. 7.2a), as opposed to the *I-V* characteristic of a rectifying contact shown in Fig. 7.2b. Figure 7.2c shows an *I-V* characteristic which is more representative of a practical ohmic contact to silicon. Although nonlinear near the origin, it develops only a small voltage across the contact at normal current levels.

Figure 7.3 shows a number of ways in which aluminum may contact semiconductor regions during device fabrication. Aluminum contact to *p*-type silicon normally results in a good ohmic contact for doping levels exceeding $10^{16}/cm^3$. However, a problem arises in trying to contact *n*-type silicon, as shown in Fig. 7.3b. For lightly doped *n*-type material, aluminum can form a metal-semiconductor "Schottky-barrier" diode rather than an ohmic contact. In order to prevent this rectifying contact from forming, an n^+ diffusion is placed between the aluminum and any lightly doped *n*-type regions, as in Fig. 7-3c. The resulting contact has an *I-V* characteristic similar to that in Fig. 7.2c. This technique was used in the bipolar process shown in Fig. 1.6.

7.2.2 Aluminum-Silicon Eutectic Behavior

Silicon melts at a temperature of 1412 °C, and pure aluminum melts at 660 °C. However, aluminum and silicon together exhibit "eutectic" characteristics in which mixture of the

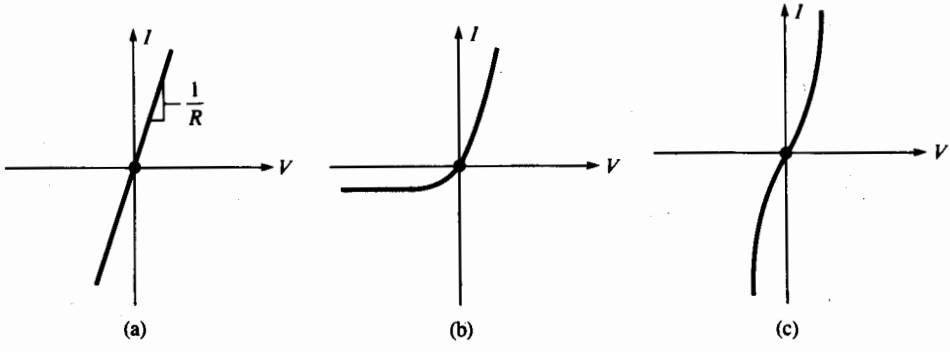

Fig. 7.2 *I-V* characteristics of contacts between integrated-circuit materials. (a) Ideal ohmic contact; (b) rectifying contact; (c) practical nonlinear "ohmic" contact.

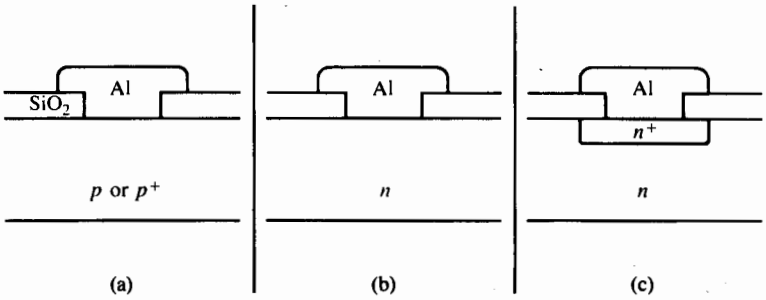

Fig. 7.3 Three possible types of aluminum contacts to silicon. (a) Aluminum to p-type silicon forms an ohmic contact with an I-V characteristic approximating that in Fig. 7.2a; (b) aluminum to n-type silicon can form a rectifying contact (Schottky barrier diode) like that in Fig. 7.2b; (c) aluminum to n^+ silicon yields a contact similar to that in Fig. 7.2c.

two materials lowers the melting point of the composite material to below that of either element. Figure 7.4 shows the phase diagram of the aluminum-silicon system at a pressure of 1 atm. The minimum melting temperature, the "eutectic temperature," is 577 °C and corresponds to a 88.7% Al, 11.3% Si composition. Because of the relatively low eutectic temperature of the Al-Si system, aluminum must be introduced into the IC process sequence after all high-temperature processing has been completed.

7.2.3 Aluminum Spiking and Junction Penetration

In order to ensure good contact formation, aluminum is normally annealed in an inert atmosphere at a temperature of 450 to 500 °C following deposition and patterning. Although this temperature is well below the eutectic temperature for silicon and aluminum, silicon still diffuses into the aluminum. The diffusion leads to a major problem associated with the formation of aluminum contacts to silicon, particularly for shallow junctions.

Anywhere a contact is made between aluminum and silicon, silicon will be absorbed by the aluminum during the annealing process. The amount of silicon absorbed will depend on the time and temperature involved in the annealing process, as well as the area of the contact (see Problem 7.4). To make matters worse, the silicon is not absorbed uniformly from the contact region. Instead, it tends to be supplied from a few points. As the silicon is dissolved, spikes of aluminum form and penetrate into the silicon contact region. If the contact is to a shallow junction, the spike may cause a junction short, as in Fig. 7.5.

The inset in Fig. 7.4 gives the solubility of silicon in aluminum. Between 400 °C and the eutectic temperature, the solubility of silicon in aluminum ranges from 0.25 to 1.5% by weight. To solve the spiking problem, silicon may be added to the aluminum film during deposition by coevaporation from two targets, or sputter deposition can be used with an aluminum target which contains approximately 1% silicon. Both of these

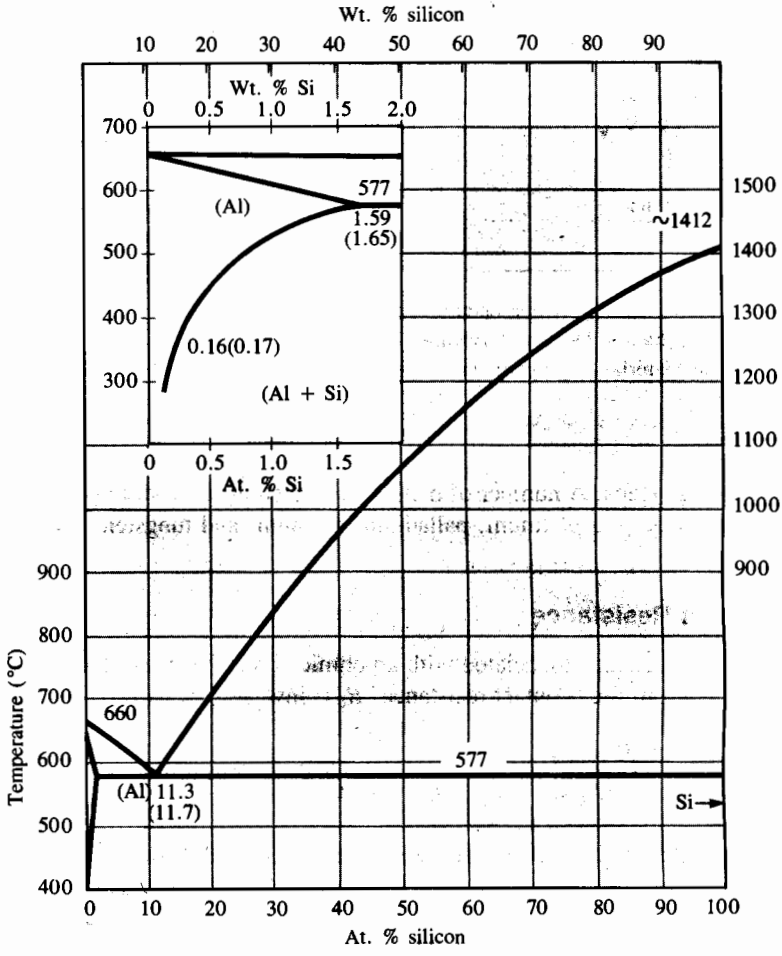

Fig. 7.4 Phase diagram of the aluminum-silicon system. The silicon-aluminum eutectic point occurs at a temperature of 577 °C. At contact-alloying temperatures between 450 and 500 °C, aluminum will absorb from 0.5 to 1% silicon. Copyright, 1958, McGraw-Hill Book Company, with permission from ref. [1].

techniques deposit a layer in which the aluminum demand for silicon is satisfied, and the metallization does not absorb silicon from the substrate during subsequent annealing steps.

Another way to prevent spiking is to place a barrier material between the aluminum and silicon, as shown in Fig. 7.5. One possibility is to deposit a thin layer of polysilicon prior to aluminum deposition. The polysilicon will then supply the silicon needed to saturate the aluminum. Another alternative is to use a metal as a barrier. The metal must form a low-resistance contact with silicon, not react with aluminum, and be compatible

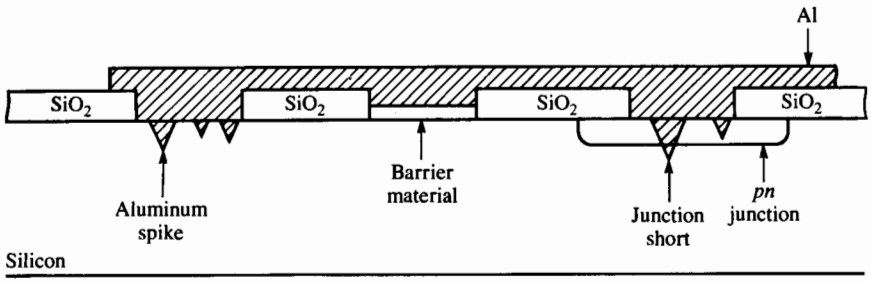

Fig. 7.5 Aluminum spiking which occurs during aluminum-silicon alloying. Aluminum spikes can cause shorts in shallow junctions. Aluminum containing 1% silicon is often used to eliminate spiking. A barrier material of polysilicon or a metal such as titanium can also be used to prevent spiking.

with other process steps. A number of metals have been used by various semiconductor manufacturers, including platinum, palladium, titanium, and tungsten.

7.2.4 Contact Resistance

There is a small resistance associated with an ohmic contact between two materials. To a first approximation, the "contact resistance" R_c is inversely proportional to the area of the contact:

$$R_c = \rho_c / A \tag{7.1}$$

where ρ_c is the specific contact resistivity in ohm-cm^2 and A is the area of the contact. For example, a 2×2 μm contact with $\rho_c = 1$ μohm-cm^2 yields a contact resistance of 25 ohms. Figure 7.6 shows the contact resistivity as a function of annealing temperature for several aluminum-silicon systems. It is evident why the 450 °C annealing process is used following aluminum deposition. Also note that the use of polysilicon under aluminum to prevent junction spiking yields a much poorer value of ρ_c.

7.2.5 Electromigration

Metal interconnections in integrated circuits are operated at relatively high current densities, and a very interesting failure mechanism develops in aluminum and other conductors. *Electromigration* is the movement of atoms in a metal film due to momentum transfer from the electrons carrying the current. Under high-current-density conditions, metal-atom movement causes voids in some regions and metal pileup or "hillocks" in other regions, as shown in Fig. 7.7. Voids can eventually result in open circuits, and pileup can cause short circuits between closely spaced conductors.

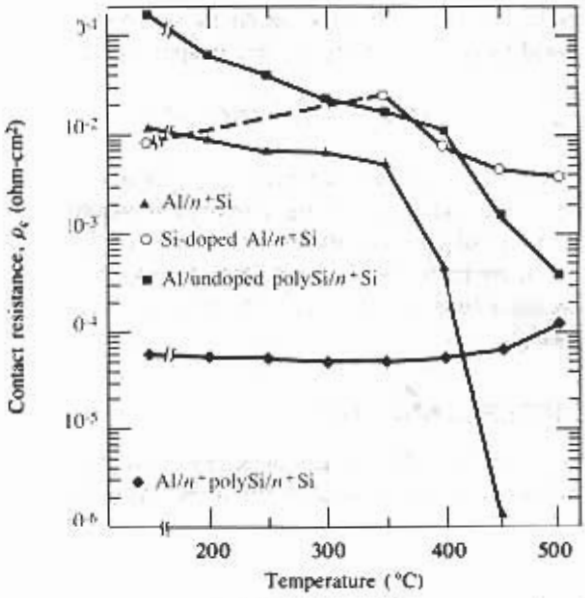

Fig. 7.6 Contact resistivity of a variety of aluminum-silicon systems. An alloying temperature of 450 °C is typically used to obtain low-contact resistance for Al-Si contacts. Reprinted with permission from *Solid-State Electronics*, Vol. 23, p. 255–262, M. Finetti et al., "Aluminum-Silicon Ohmic Contact on Shallow n^+/p Junctions," Copyright 1980, Pergamon Press, Ltd.

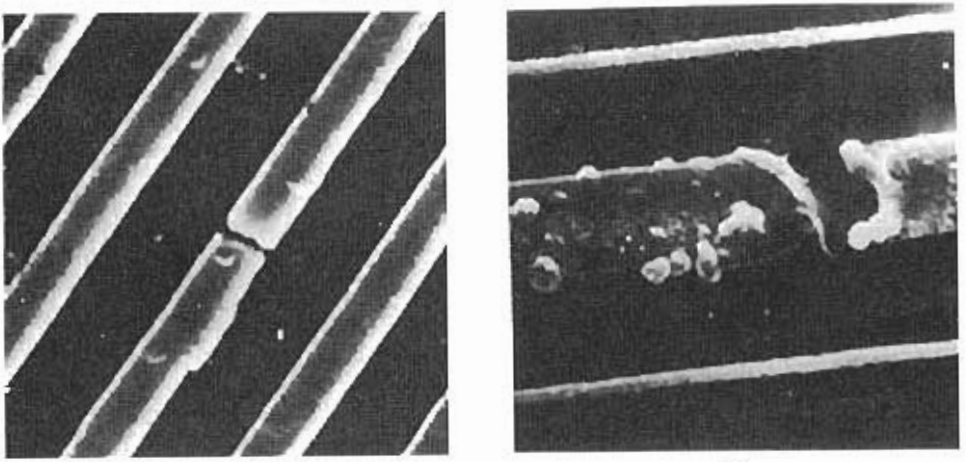

Fig. 7.7 Scanning electron micrographs of aluminum interconnection failure caused by electromigration. (a) Sputtered aluminum with 0.5% copper; (b) evaporated aluminum with 0.5% copper. Copyright, 1980, IEEE. Reprinted with permission from ref. [3].

The mean time to failure (MTF) of a conductor due to electromigration has been experimentally related to current density, J, and temperature by

$$\text{MTF} \propto (J^{-2}) \exp(E_A/kT) \tag{7.2}$$

where E_A is an activation energy with a typical value of 0.4 to 0.5 eV for aluminum.

The most common method of improving aluminum resistance to electromigration is to add a small percentage of a heavier metal such as copper. Targets composed of 95% Al, 4% Cu, and 1% Si are routinely used in sputter deposition systems. The aluminum-copper-silicon alloy films simultaneously provide electromigration resistance and eliminate aluminum spiking.

7.3 DIFFUSED INTERCONNECTIONS

Diffused conductors with low sheet resistances represent the second available interconnect medium in basic integrated-circuit technology. From Fig. 4.16 we can see that the minimum resistivity is approximately 1000 μohm-cm. For shallow structures measuring about 1 μm, the minimum obtainable sheet resistance is typically between 10 and 20 ohms per square. Such sheet resistances are obviously much higher than that of metal, and one must be selective in the use of diffusions for signal or power distribution.

The diffused line must really be modeled as a distributed RC structure, illustrated in Fig. 7.8, when signal propagation is considered. The resistance, R, of diffused regions was discussed in detail in Chapter 4, and C represents capacitance of the reverse-biased

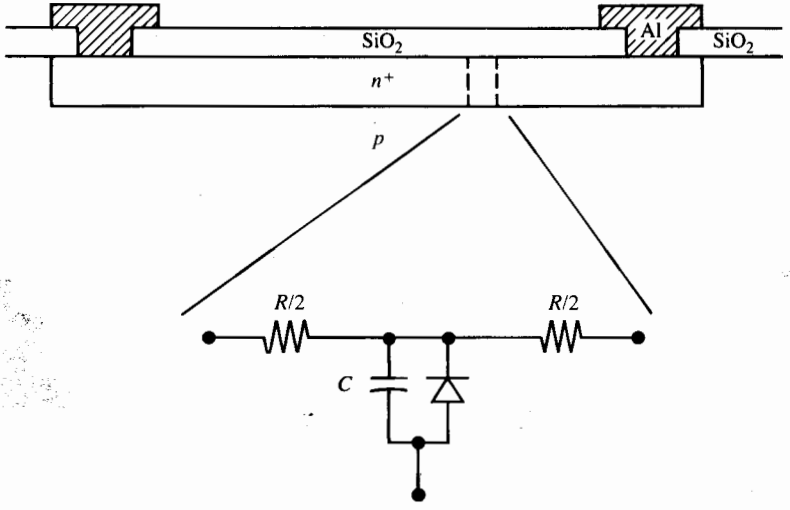

Fig. 7.8 A lumped circuit model for a small section of an n^+ diffusion. The RC line delay limits the use of diffusions for high-speed signal distribution.

pn junction formed between the diffused region and the substrate. Heavily doped diffusions are normally used for interconnection purposes and can be approximated by a one-sided step junction in which the depletion layer extends predominantly into the substrate. The capacitance per unit area is given by

$$C = \sqrt{\frac{qN_S K_s \varepsilon_0}{2(\phi_{bi} + V_R)}} \qquad \phi_{bi} = (kT/q) \ln\left(\frac{N_S}{n}\right) + 0.56 \text{ V} \qquad (7.3)$$

where N_S is the substrate doping, ϕ_{bi} is the built-in potential of the junction, and V_R is the reverse bias applied to the junction.

The relatively large *RC* product of long diffused lines results in substantial time delay for signals propagating down such a line. Hence, diffusions are more useful in interconnecting adjacent devices in integrated circuits. Figure 7.9 shows a three-input NMOS NOR-gate in which the source diffusions of the three input transistors are merged together as one diffusion. The three drains of the input devices, as well as the source of the depletion-mode load device, are also merged together as one diffusion. Figure 7.1 shows an example of the use of long diffused interconnection regions in a programmable-logic-array (PLA) structure.

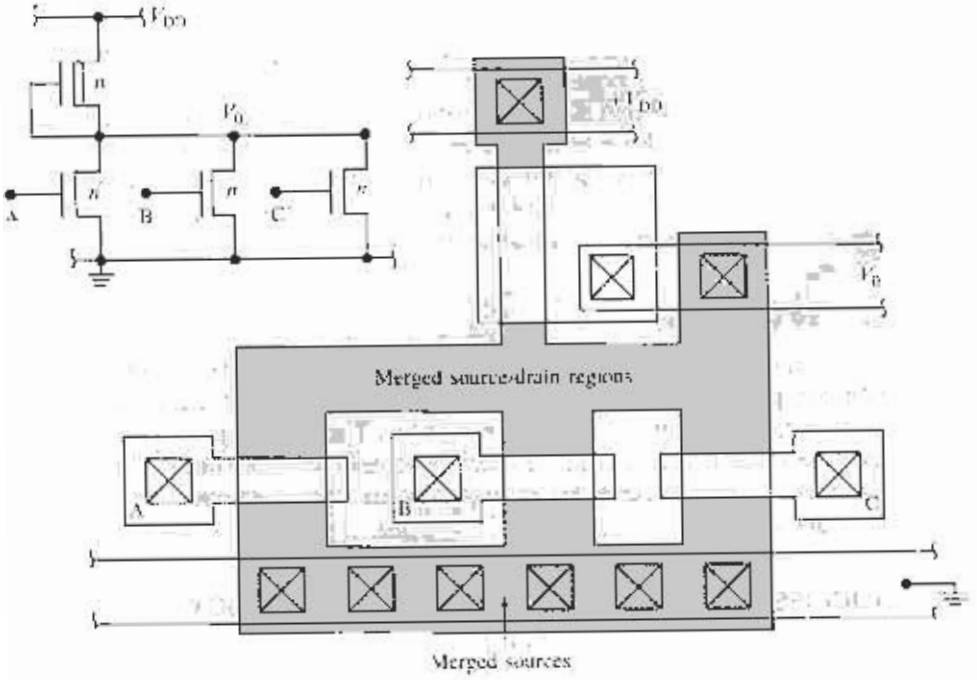

Fig. 7.9 Layout of an NMOS NOR-gate showing device interconnection through merging of adjacent source and drain diffusions.

7.4 POLYSILICON INTERCONNECTIONS AND BURIED CONTACTS

Heavily doped *n*-type polysilicon is the primary MOS transistor gate material in use today, and it provides an additional layer of interconnection which is easily insulated from other layers by thermal oxidation or insulator deposition. This extra level of interconnection greatly facilitates the layout of compact digital integrated circuits. Thin, heavily doped polysilicon layers have a minimum resistivity of approximately 300 μohm-cm, and they suffer from the same sheet-resistance problems associated with shallow diffused interconnections (typically 20 to 30 ohms per square). Polysilicon lines have substantial capacitance to the substrate and exhibit *RC* delay problems similar to those of diffused interconnections.

7.4.1 Buried Contacts

In the polysilicon-gate processes presented thus far, the polysilicon acts as a barrier material during ion implantation or diffusion. Thus, a diffusion can never pass beneath a polysilicon line. In addition, contact windows to the diffusions are not opened until after polysilicon deposition. It is therefore necessary to use a metal link to connect between polysilicon and diffusion, as in Fig. 7.10a. Interconnecting the diffusion to polysilicon in this manner requires two contact windows and an intervening space, both of which are wasteful of area.

In memory arrays, where density is extremely important, an extra mask step can be introduced into the process to permit direct contact between polysilicon and silicon, as shown in Fig. 7.10b. Prior to polysilicon deposition, windows are opened in the thin gate oxide, permitting the polysilicon to contact the silicon surface. Diffusion of the *n*-type dopant from the heavily doped n^+ polysilicon merges with the adjacent ion-implanted n^+ regions, and the result is called a *buried contact*. The edge of the contact exhibits the lowest resistance since the impurity concentration is greatest in that region.

7.4.2 Butted Contacts

Another method of conserving area is to form a "butted" contact as shown in Fig. 7.10c. In this example, polysilicon is aligned with the edge of the diffusion contact window, and metal connects the diffusion and polysilicon together. The butted contact saves area by eliminating the space normally required between separate contact windows. However, some manufacturers do not use butted contacts because of concern about the reliability of such contacts.

7.5 SILICIDES AND MULTILAYER-CONTACT TECHNOLOGY

The sheet resistance of both thin polysilicon and shallow diffusions cannot be reduced below 10 to 20 ohms per square, which greatly reduces their utility as an interconnection medium. Interconnect delays are beginning to limit the speed of VLSI circuits, and as

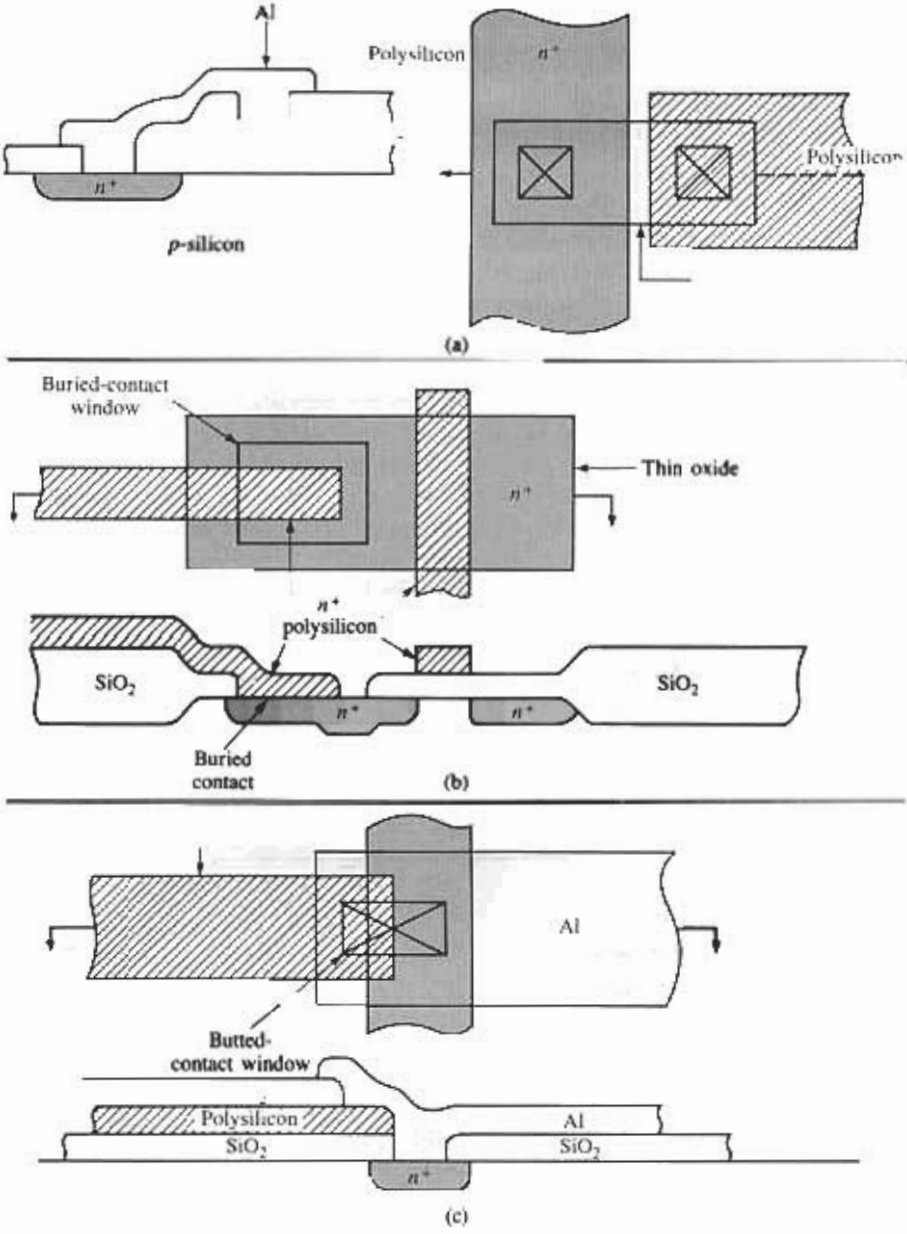

Fig. 7.10 Three techniques for interconnecting polysilicon and n^+ diffusion. (a) Normal aluminum link requiring two contact regions and an intervening space; (b) buried-contact structure; (c) butted-contact structure.

dice get larger and feature sizes get smaller, methods for improving these interconnections have had to be found.

7.5.1 Silicides, Polycides, and Salicides

A wide range of noble and refractory metals form compounds with silicon called *silicides,* and the sheet resistance of polysilicon and diffusion can be reduced by forming a low-resistivity, shunting silicide layer on their surfaces. A list of properties of possible silicides is given in Table 7.1. Several of the elements, including titanium, tungsten, platinum, and palladium, have been used in the formation of Schottky-barrier diodes in bipolar processes since the 1960s and are now used to form silicides for interconnection purposes.

A structure with a silicide formed on top of the polysilicon gate, often called a *polycide,* is shown in Fig. 7.11. A layer of the desired metal is deposited using evaporation, sputtering, or CVD techniques. Upon heating of the structure to a temperature between 600 and 1000 °C, the metal reacts with the polysilicon to form the desired silicide. Coevaporation, cosputtering, or sputtering of a composite target may be used to simultaneously deposit both silicon and metal onto the polysilicon surface prior to the thermal treatment or "sintering" step. Silicides have resistivities in the range of 15 to 50 μohm-cm.

Table 7.1 Properties of Some Silicides of Interest. Reprinted with permission of the American Institute of Physics from ref. [4].

Silicide	Starting Form	Sintering Temperature (°C)	Lowest Binary Eutectic Temperature (°C)	Specific Resistivity (μohm-cm)
$CoSi_2$	Metal on polysilicon	900	1195	18–25
	Cosputtered alloy	900		
$HfSi_2$	Metal on polysilicon	900	1300	45–50
$MoSi_2$	Cosputtered alloy	1000	1410	100
$NiSi_2$	Metal on polysilicon	900	966	50
	Cosputtered alloy	900		50–60
Pd_2Si	Metal on polysilicon	400	720	30–50
PtSi	Metal on polysilicon	600–800	830	28–35
$TaSi_2$	Metal on polysilicon	1000	1385	35–45
	Cosputtered alloy	1000		50–55
$TiSi_2$	Metal on polysilicon	900	1330	13–16
	Cosputtered alloy	900		25
WSi_2	Cosputtered alloy	1000	1440	70
$ZrSi_2$	Metal on polysilicon	900	1355	35–40

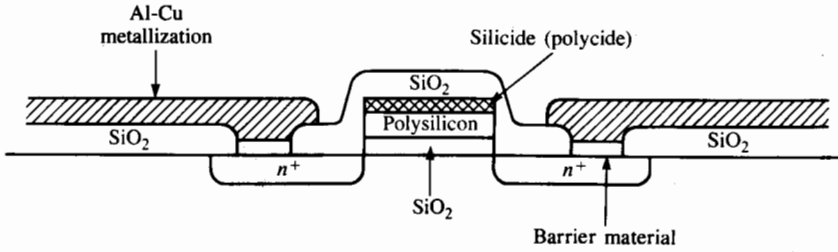

Fig. 7.11 MOS structure showing the use of a "polycide" to reduce the sheet resistance of the polysilicon gate material and a barrier material to prevent aluminum spiking through shallow source/drain junctions.

Another feature of silicide layers is the ability to oxidize the surface following silicide formation. At high temperature, silicon diffuses readily through the silicide layer and will combine with oxygen at the silicide surface to form an SiO_2 insulating layer.

The eutectic temperature of the silicide and silicon will limit the temperature of further processing steps, as in the case of aluminum. However, many silicides are stable at temperatures exceeding 1000 °C. Exceptions include the silicides of nickel (900 °C), platinum (800 °C), and palladium (700 °C).

Silicides are also used to reduce the effective sheet resistance of diffused interconnections. Figure 7.12 outlines a process for simultaneous formation of silicides on both the gate and source/drain regions of an MOS transistor. An oxide spacer is used to prevent silicide formation on the side of the gate, because such formation could cause a short between the gate and diffusions. The spacer is formed by first coating the surface with a CVD oxide, followed by a reactive-ion etching step. The oxide along the edge of the gate is thicker than over other regions, and some oxide is left on the side of the gate at the point when the oxide is completely removed from the source and drain regions and the top of the gate. Next, metal is deposited over the wafer. During sintering, silicide forms only in the regions where metal touches silicon or polysilicon. Unreacted metal may be removed with a selective etch which does not attack the silicide. The result is a silicide that is automatically self-aligned to the gate and source/drain regions. *Self-aligned silicides* are often called *salicides*.

7.5.2 Barrier Metals and Multilayer Contacts

Aluminum contacts to silicides suffer from the same pitting and spiking problems associated with direct contact to silicon. To circumvent these problems, an intermediate layer of metal is used that prevents silicon diffusion. Figure 7.13 shows the application of titanium-tungsten, TiW, as a barrier metal over the silicides in the contact regions of both bipolar and MOS technologies. The final contact consists of a sandwich of a silicide over the diffusion, followed by the TiW diffusion barrier, and completed with aluminum-copper interconnection metallization. Multilayer contact structures are becoming quite common in high-density, high-performance MOS and bipolar technologies.

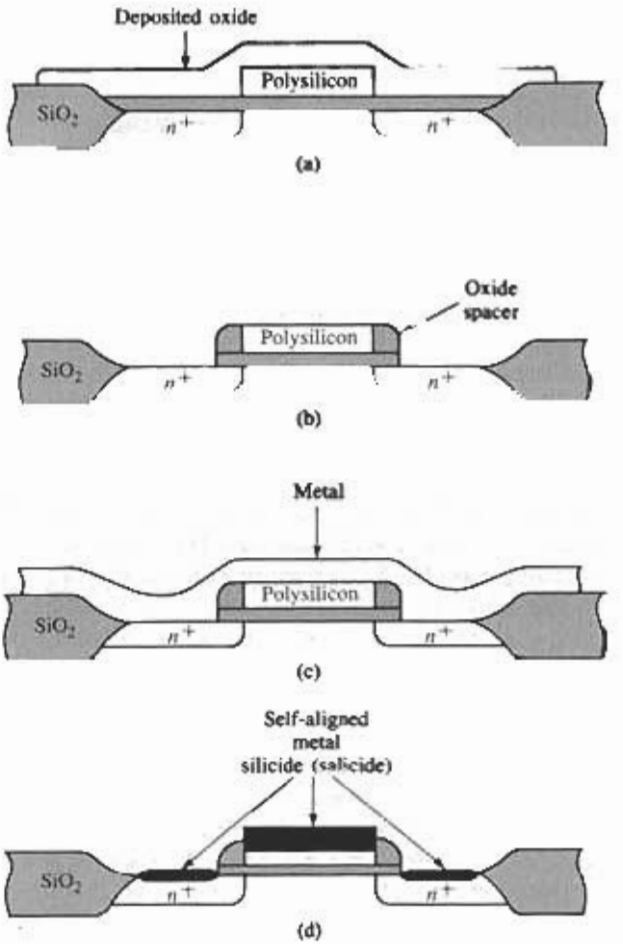

Fig. 7.12 Use of a self-aligned silicide ("salicide") in the formation of a MOS device. (a) Oxide is deposited over the normal MOS structure following polysilicon definition; (b) structure after reactive-ion etching leaving a sidewall oxide spacer; (c) metal is deposited over the structure and heated to form silicides; (d) unreacted metal is readily etched away, leaving silicide automatically aligned to gate and source/drain regions.

7.6 THE LIFTOFF PROCESS

The pattern definition processes which have been discussed previously have been "subtractive" processes, as illustrated in Fig. 7.14a. The wafer is completely covered with a thin film layer, which is selectively protected with a masking layer such as photoresist. Wet or dry etching then removes the thin film material from the unprotected areas

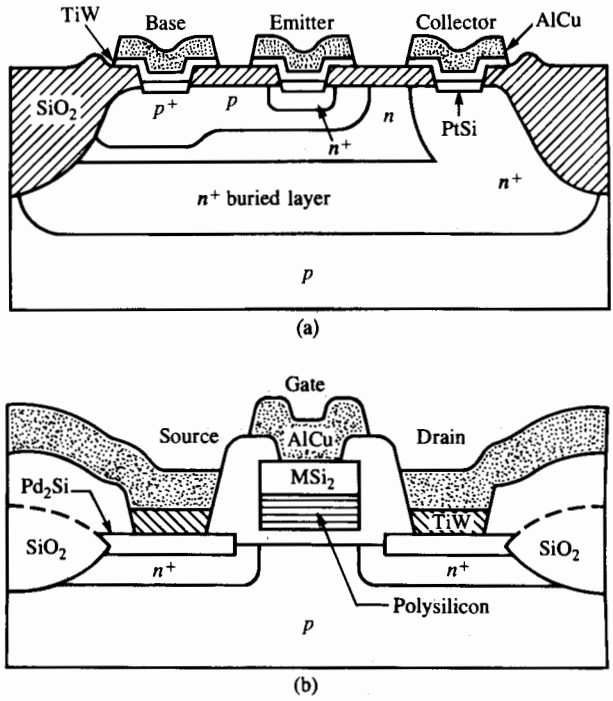

Fig. 7.13 Device cross sections showing the use of silicide contacts in (a) bipolar and (b) MOS devices. Reprinted with permission from Semiconductor International magazine, August 1985.[5] Copyright 1985 by Cahners Publishing Co., Des Plaines, IL.

The additive or *liftoff* process shown in Fig. 7.14b can also be used, in which the substrate is first covered with a photoresist layer patterned with openings where the final material is to appear. The thin film layer is deposited over the surface of the wafer. Any material deposited on top of the photoresist layer will be removed with the resist, leaving the patterned material on the substrate. For liftoff to work properly, there must be a very thin region or a gap between the upper and lower films. Otherwise tearing and incomplete liftoff will occur.

The masking patterns for the liftoff and subtractive processes are the negatives of each other. This can be achieved by changing the mask from dark field to light field or by changing from negative to positive photoresist.

7.7 MULTILEVEL METALLIZATION

A single level of metal simply does not provide sufficient capability to fully interconnect complex VLSI chips. Many processes now use two or three levels of polysilicon as well

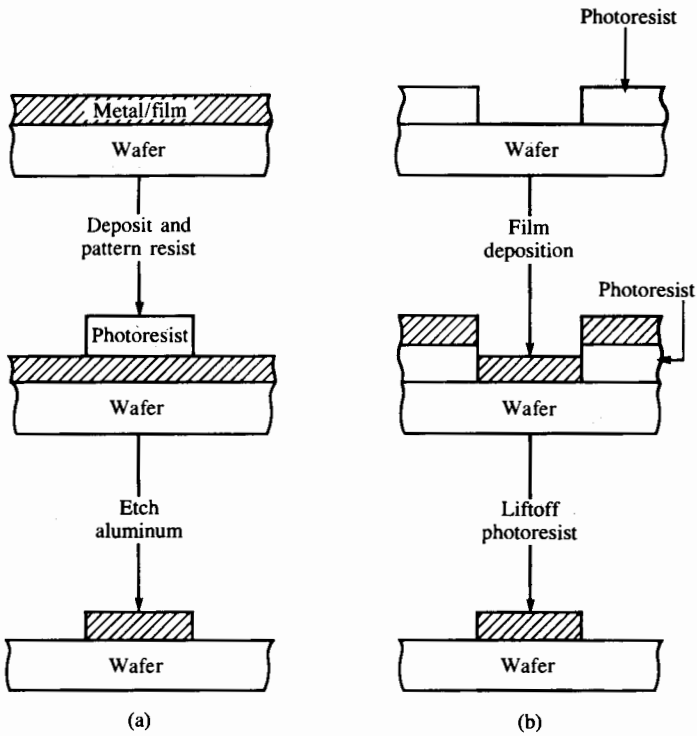

Fig. 7.14 A comparison of interconnection formation by (a) subtractive etching and (b) additive metal liftoff.

as several levels of metallization in order to ensure wirability and provide adequate power distribution.

A multilevel metal system is shown in Fig. 7.15. Standard processing is used through the deposition and patterning of the first level of metal. An interlevel dielectric, consisting of CVD or sputtered SiO_2, or a plastic-like material called *polyimide*, is then deposited over the first metal layer. The dielectric layer must provide good step coverage and should help smooth the topology. In addition, the layer must be free of pinholes and be a good insulator.

Next, vias are opened in the dielectric layer, and the second level of metallization is deposited and patterned. In the process in Fig. 7.15b, a via filling technique, which improves the overall topology, is used prior to deposition of each metal level. The dielectric deposition and metallization processes are repeated until the desired number of levels of interconnection are achieved. Integrated circuits with up to four levels of metal have been successfully fabricated using similar processes.

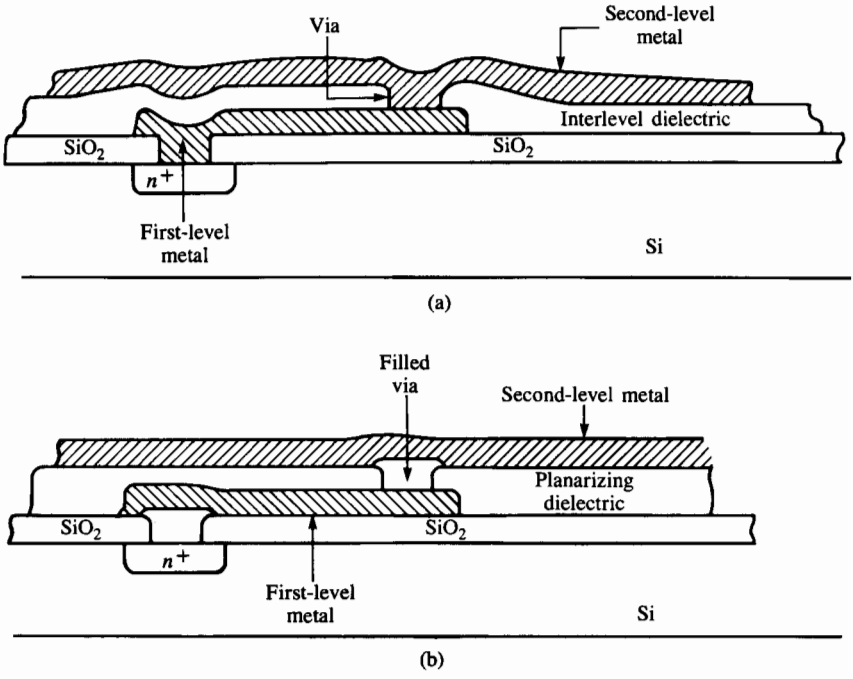

Fig. 7.15 (a) Basic two-level metallization process may use polyimide, oxide, or nitride as an interlevel dielectric; (b) additional process steps may be added to fill the vias with metal prior to each metal deposition in order to achieve a more planar structure.

7.8 SUMMARY

In this chapter we have explored the various types of interconnections used in modern integrated circuits, including diffusion, polysilicon, and metal. Diffusion and polysilicon have a relatively high sheet resistance, which often restricts their use to local interconnections. The formation of metal silicides on the surface of polysilicon lines and diffusions can substantially reduce the sheet resistance of these interconnections.

Problems relating to the formation of good ohmic contacts between aluminum and silicon have also been discussed. An n^+ layer is required between aluminum and n-type silicon to prevent formation of a Schottky-barrier diode instead of an ohmic contact. Aluminum penetration into silicon is a serious problem in forming contacts to shallow junctions. Metals such as tungsten and titanium are often used as silicon diffusion barriers to prevent aluminum penetration into contacts to silicon or silicides.

At high current densities, a failure mechanism called *electromigration* can cause open and short circuits to form in the metallization layers. Aluminum containing approxi-

mately 1% silicon and 4% copper is used to minimize aluminum spiking and electromigration, respectively.

Multilevel metal processes have been developed for integrated circuits which require more than one level of metallization. Some of today's processes contain up to three levels of polysilicon, and others use four levels of metallization.

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PROBLEMS

7.1 (a) What is the sheet resistance of a 1-μm-thick aluminum-copper-silicon line with a resistivity of 3.2 μohm-cm?

(b) What would be the resistance of a line 500 μm long and 10 μm wide?

(c) What is the capacitance of this line to the substrate if it is on an oxide which is 1 μm thick? (Assume that you can use the parallel-plate capacitance formula).

(d) What is the RC product associated with this 500-μm line?

7.2 (a) Repeat Problem 7.1 for a polysilicon line with a resistivity of 500 μohm-cm.

(b) Repeat Problem 7.1 for a titanium silicide line with a resistivity of 25 μohm-cm.

7.3 (a) Compute estimates of the sheet resistance of shallow arsenic and boron diffusions by assuming uniformly doped rectangular regions with the maximum achievable electrically active impurity concentrations (see Fig. 4.6). Use hole and electron mobilities of 75 and 100 cm^2/V-sec, respectively, and a depth of 0.25 μm.

(b) Compare your answers with those for diffused lines obtained from Figs. 4.6 and 4.16. Use the maximum possible electrically active concentration for the boron and arsenic surface concentrations.

7.4 Suppose that a 500 × 15 μm aluminum line makes contact with silicon through a 10 × 10 μm contact window as shown in Fig. P7.4. The aluminum is 1 μm thick and is annealed at 450 °C for 30 min. Assume that the silicon will saturate the aluminum up to a distance $\sqrt{Dt}$ from the contact. D is the diffusion coefficient of silicon in aluminum which follows an Arrhenius relationship with $D = 0.04$ cm^2/sec and $E_A = 0.92$ eV. Assume that silicon is absorbed uniformly through the contact and that the density of aluminum and silicon is the same. How deep will the aluminum penetration into the silicon be?

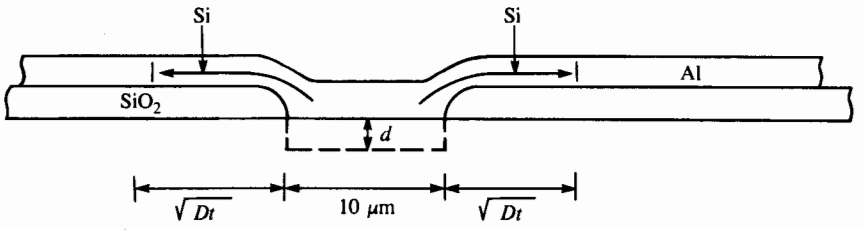

Fig. P7.4

7.5 A certain process forms aluminum contacts to n^+ silicon through a 10 × 10 μm contact window resulting in a contact resistance of 0.5 ohms.

(a) What is the specific contact resistivity for this contact?

(b) What will the contact resistance be if the contact windows are reduced to 1 × 1 μm? Does this seem acceptable for a VLSI process?

7.6 Electromigration failures depend exponentially on temperature.

(a) What is the ratio of the MTFs of identical aluminum conductors operating at the same current density at 300 K and 400 K?

(b) At 77 K, (liquid-nitrogen temperature) and 400 K? Use $E_A = 0.5$ eV.

7.7 An n^+ diffusion is used for interconnection. The surface concentration of the diffusion is $4 \times 10^{19}/cm^3$ and the junction depth is 4 μm. The diffusion is formed in a p-type wafer with a background concentration of $1 \times 10^{15}/cm^3$.

(a) What is the sheet resistance of this diffusion?

(b) Estimate the capacitance per unit length if the diffusion is 15 μm wide. Assume the rectangular geometry shown in Fig. P7.7 and use the step-junction-capacitance formula.

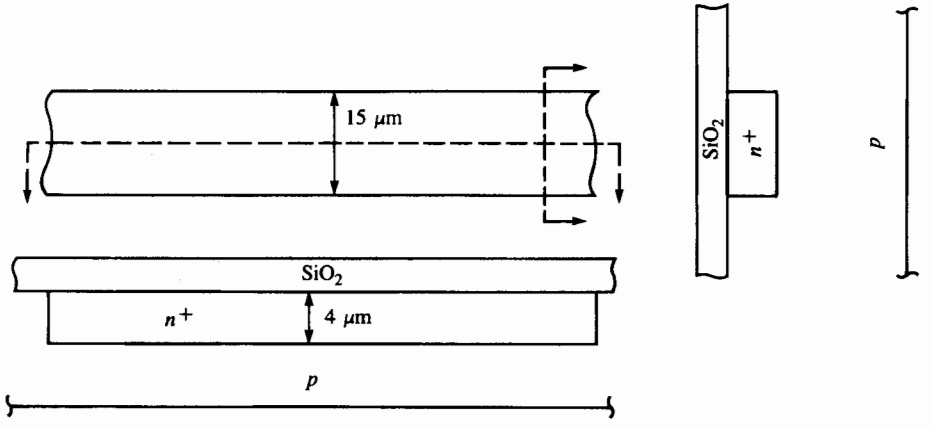

Fig. P7.7

7.8 What is the maximum current that may be allowed to flow in an aluminum conductor 1 μm thick and 4 μm wide if the current density must not exceed 5×10^5 A/cm^2?